IBM System z

Introducing the IBM® **z13**™ Server

Platform Structure and Performance

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January 2015

IBM

Agenda

- Design Imperatives
- The IBM z Systems z13 Server
- The z13 Big Data Server

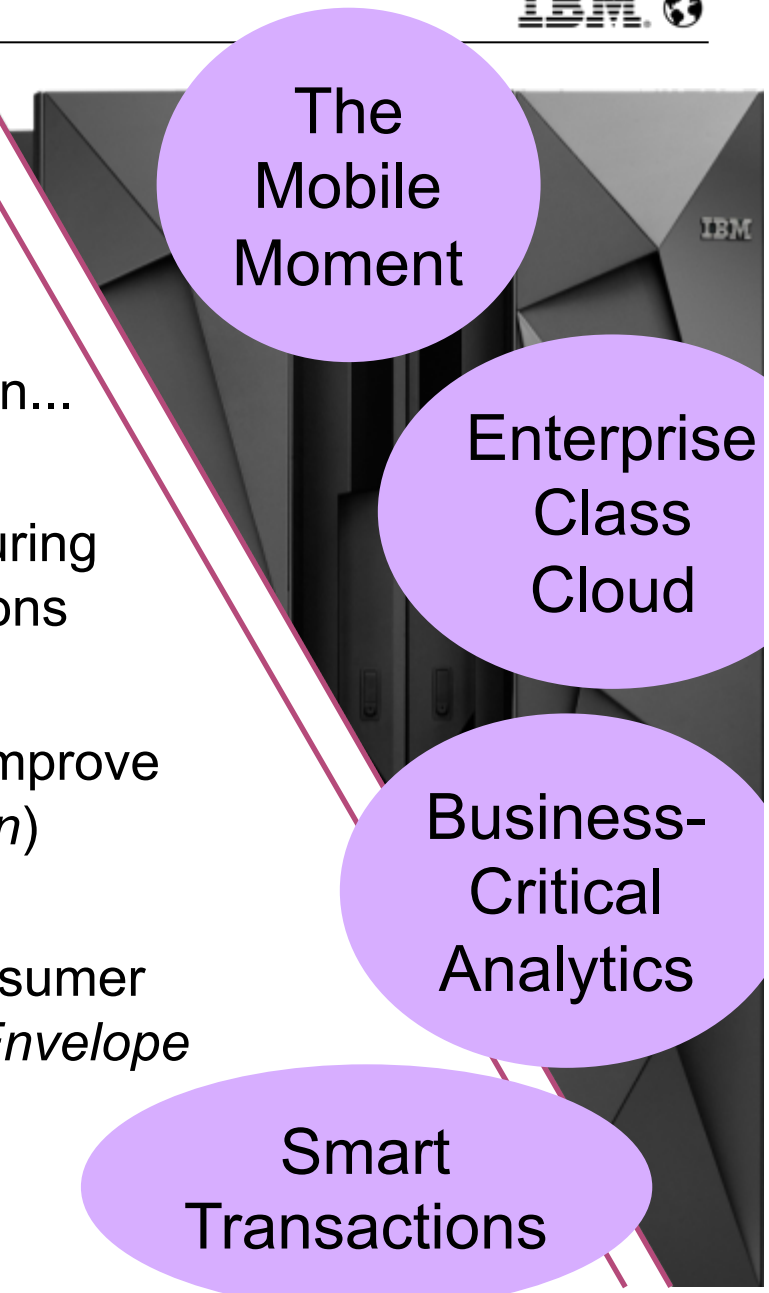
Design Imperatives

Business Imperatives

The Odds are High …

Business Management is interested in...

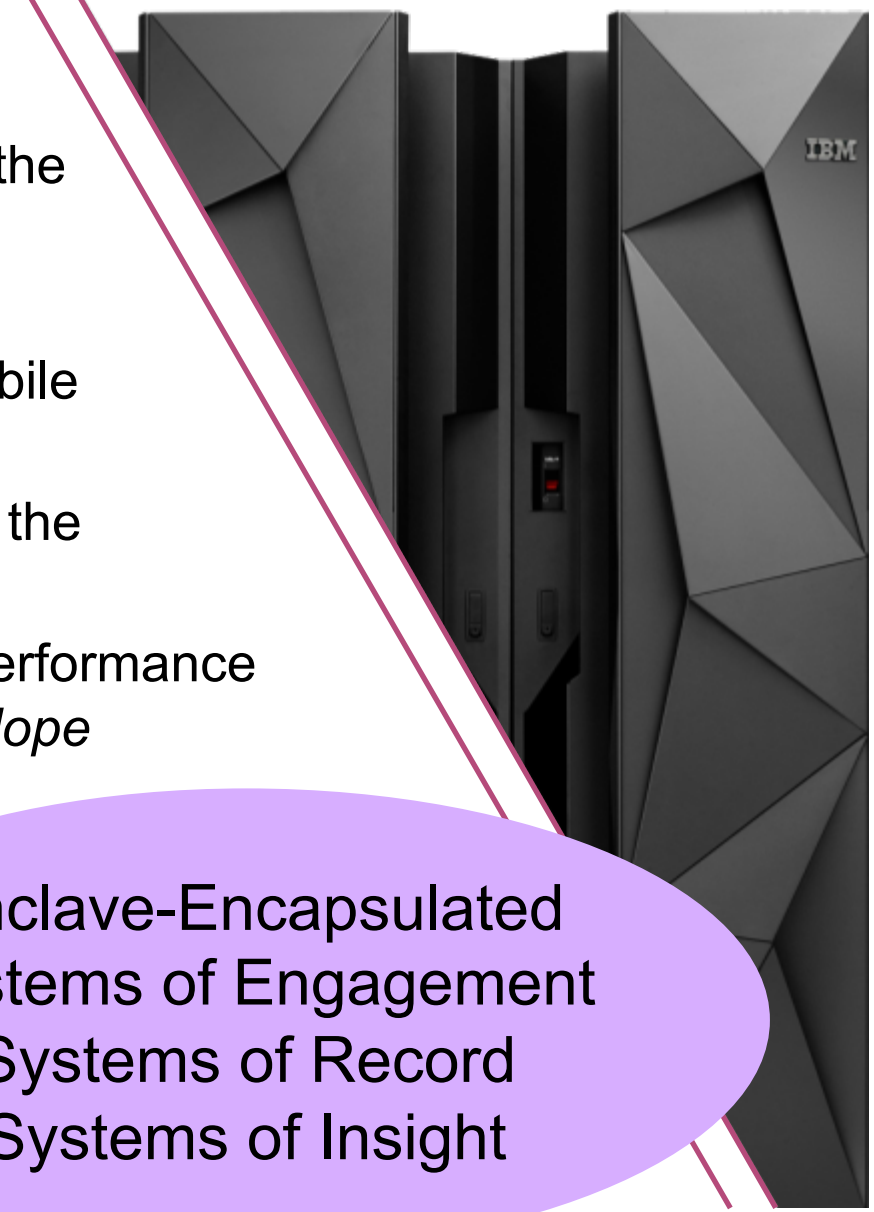
- Promoting High Retention Rates and Capturing Competitive share through mobile interactions
- Driving integrated/smart transactions that improve the Client Experience (e.g. *Next Best Action*)
- Growing and Improving the IT services consumer experience within *Existing Environmental Envelope*



IBM **z13** Design Primitives

The IBM **z13** Server was developed with the intent to:

- Capture transaction growth through mobile enablement of existing systems
- Drive integrated analytics at the time of the transaction
- Deliver higher levels of Capacity and Performance within the *Existing Environmental Envelope*

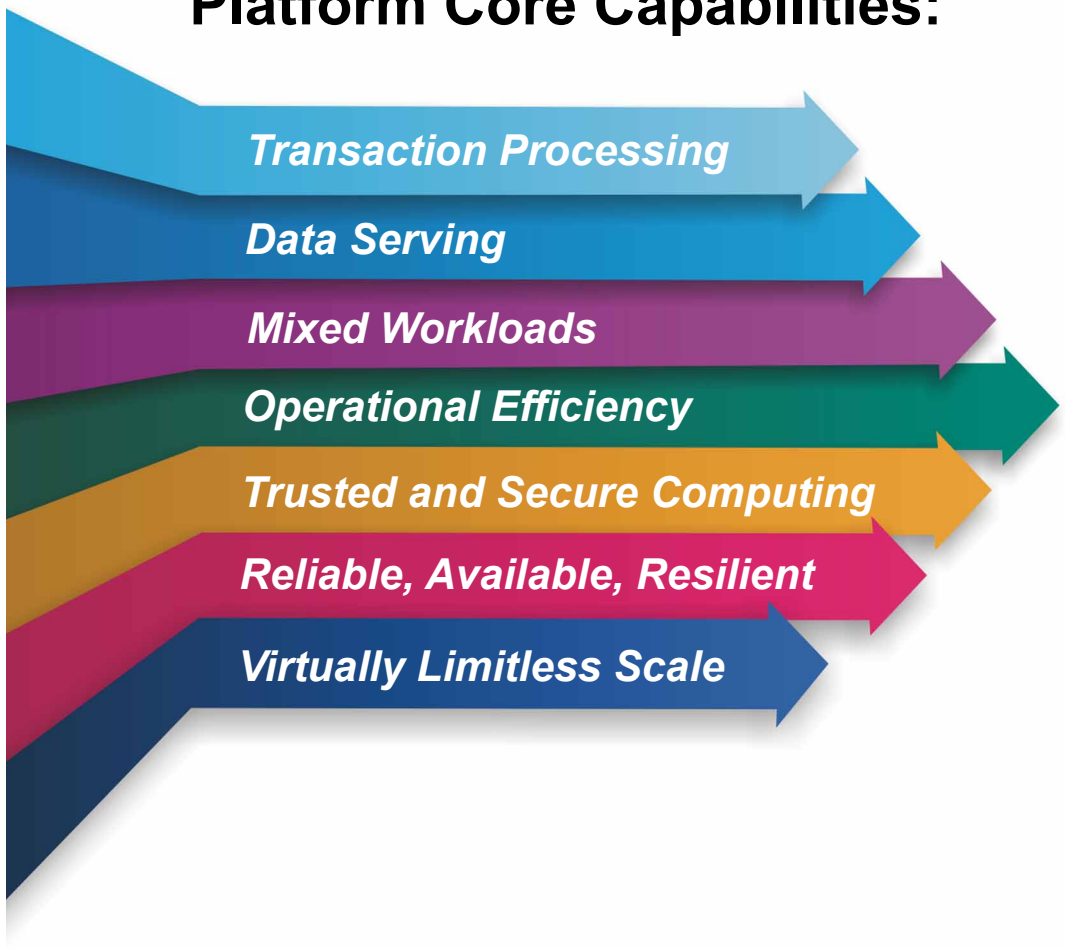


Enclave-Encapsulated
Systems of Engagement
Systems of Record
Systems of Insight

The **IBM z13** Server

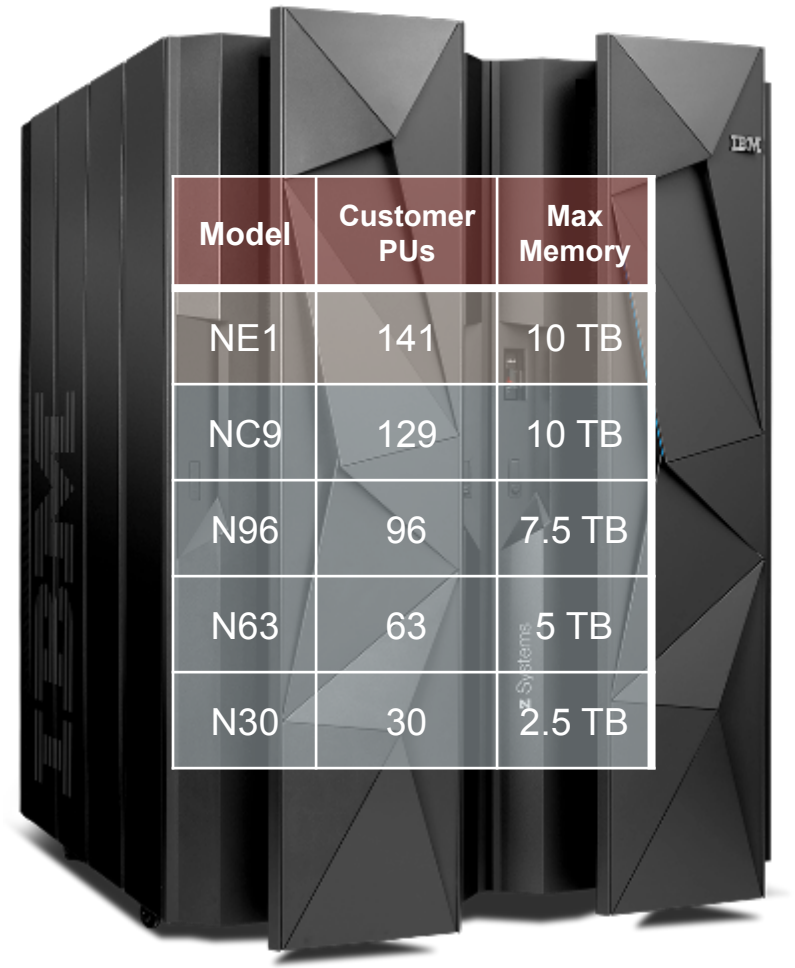
IBM z13 platform positioning

Platform Core Capabilities:



- *The world's premier transaction and data engine now enabled for the **mobile** generation*
- *The integrated transaction and **analytics** system for right-time insights at the point of impact*
- *The world's most efficient and trusted **cloud** system that transforms the economics of IT*

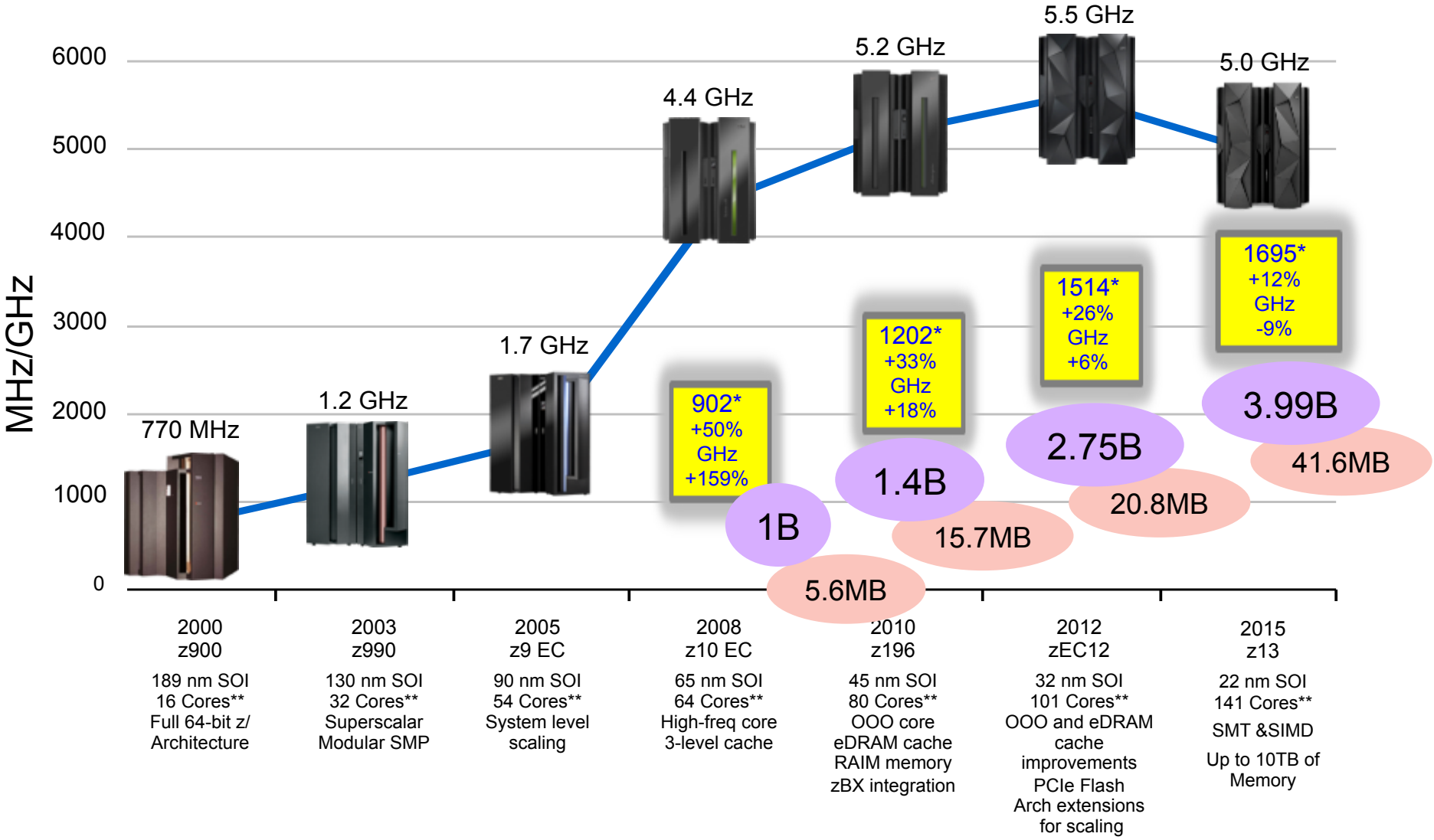
z13 Overview



Model	Customer PUs	Max Memory
NE1	141	10 TB
NC9	129	10 TB
N96	96	7.5 TB
N63	63	5 TB
N30	30	2.5 TB

- **Machine Type**
  - 2964
- **5 Models**
  - N30, N63, N96, NC9 and NE1
- **Processor Units (PUs)**
  - 39 (42 for NE1) PU cores per CPC drawer
  - Up to 24 SAPs per system, standard
  - 2 spares designated per system
  - Dependant on the H/W model - up to 30, 63, 96, 129,141 PU cores available for characterization
    - Central Processors (CPs), Internal Coupling Facility (ICFs), Integrated Facility for Linux (IFLs), IBM z Integrated Information Processor (zIIP), optional - additional System Assist Processors (SAPs) and Integrated Firmware Processor (IFP)
    - 85 LPARs, increased from 60
  - Sub-capacity available for up to 30 CPs
    - 3 sub-capacity points
- **Memory**
  - RAIM Memory design
  - System Minimum of 64 GB
  - Up to 2.5 TB GB per drawer
  - Up to 10 TB for System and up to 10 TB per LPAR (OS dependant)
    - LPAR support of the full memory enabled
    - 96 GB Fixed HSA, standard
    - 32/64/96/128/256/512 GB increments
  - Flash Express
- **I/O**
  - 6 GBps I/O Interconnects – carry forward only
  - Up to 40 PCIe Gen3 Fanouts @ 16 GBps each and Integrated Coupling Adapters @ 2 x 8 GBps per System
  - 6 Logical Channel Subsystems (LCSSs)
    - 4 Sub-channel sets per LCSS
- **Server Time Protocol** (STP)

z13 Continues the CMOS Mainframe Heritage Begun in 1994



* MIPS Tables are NOT adequate for making comparisons of z Systems processors. Additional capacity planning required
** Number of PU cores for customer use

z13@5.0GHz vs. zEC12@5.5GHz

Instruction-Set Instructions
SIMD(z13) vs. no SIMD(zEC12)

Memory Fetch Instructions
42MB/core(z13) vs 21MB/core(zEC12)

$$\frac{\text{Instructions}}{\text{Workload}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}} = \frac{\text{Seconds}}{\text{Workload}}$$

OoOX and RISC-like CISC
6 instructions/cycle(z13) vs. 3 instructions/cycle(zEC12)

zEC12 Core

CP

SAP

ICF

IFL

zIIP

zAAP

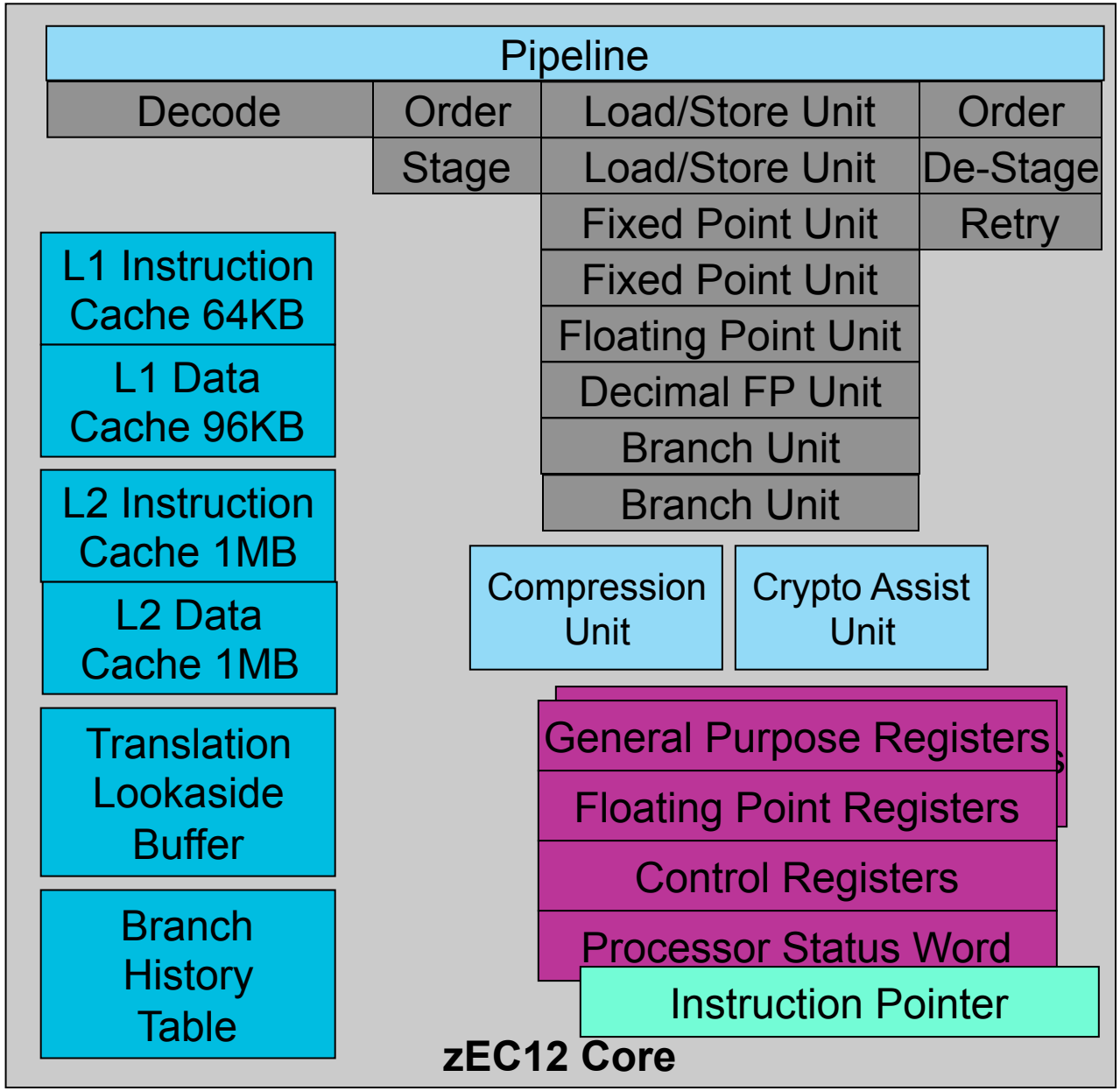
1500 to 1650 MIPS

5.5GHz

Out of Order

23 New Instr.

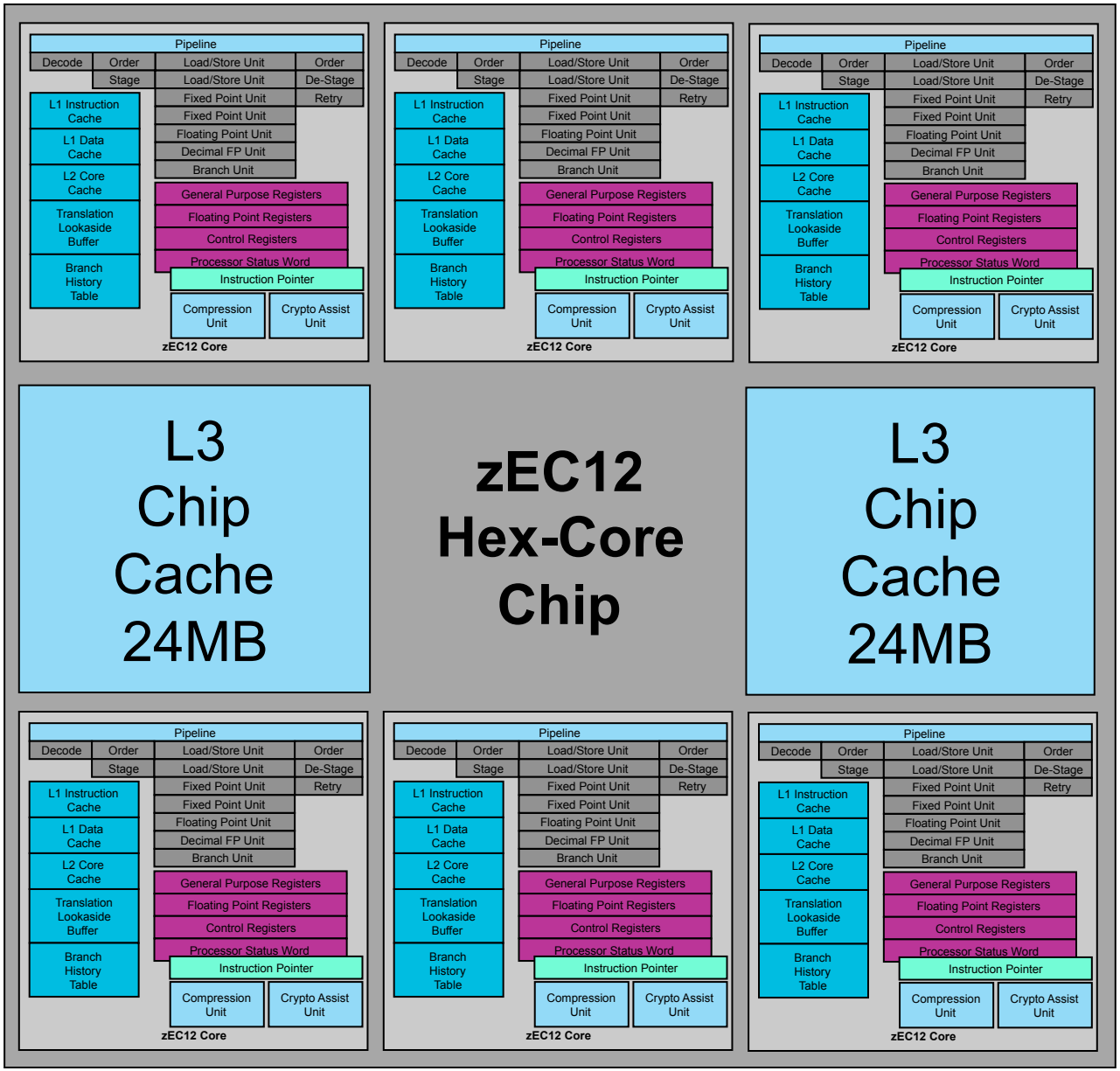
3 Instr. Per Cycle



zEC12 Chip

2.75B Transistors

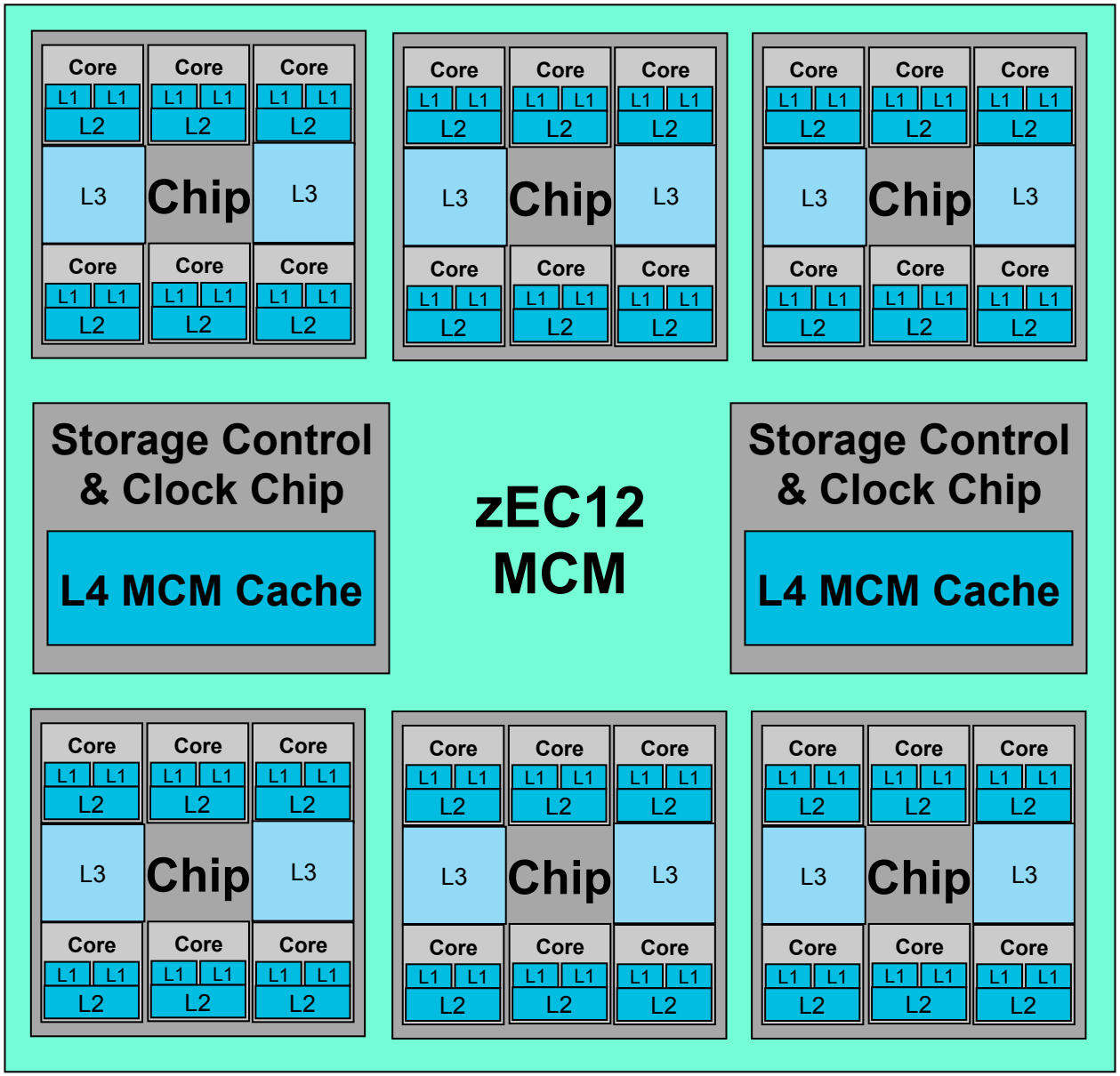
L1/L2/L3 Total 61MB cache



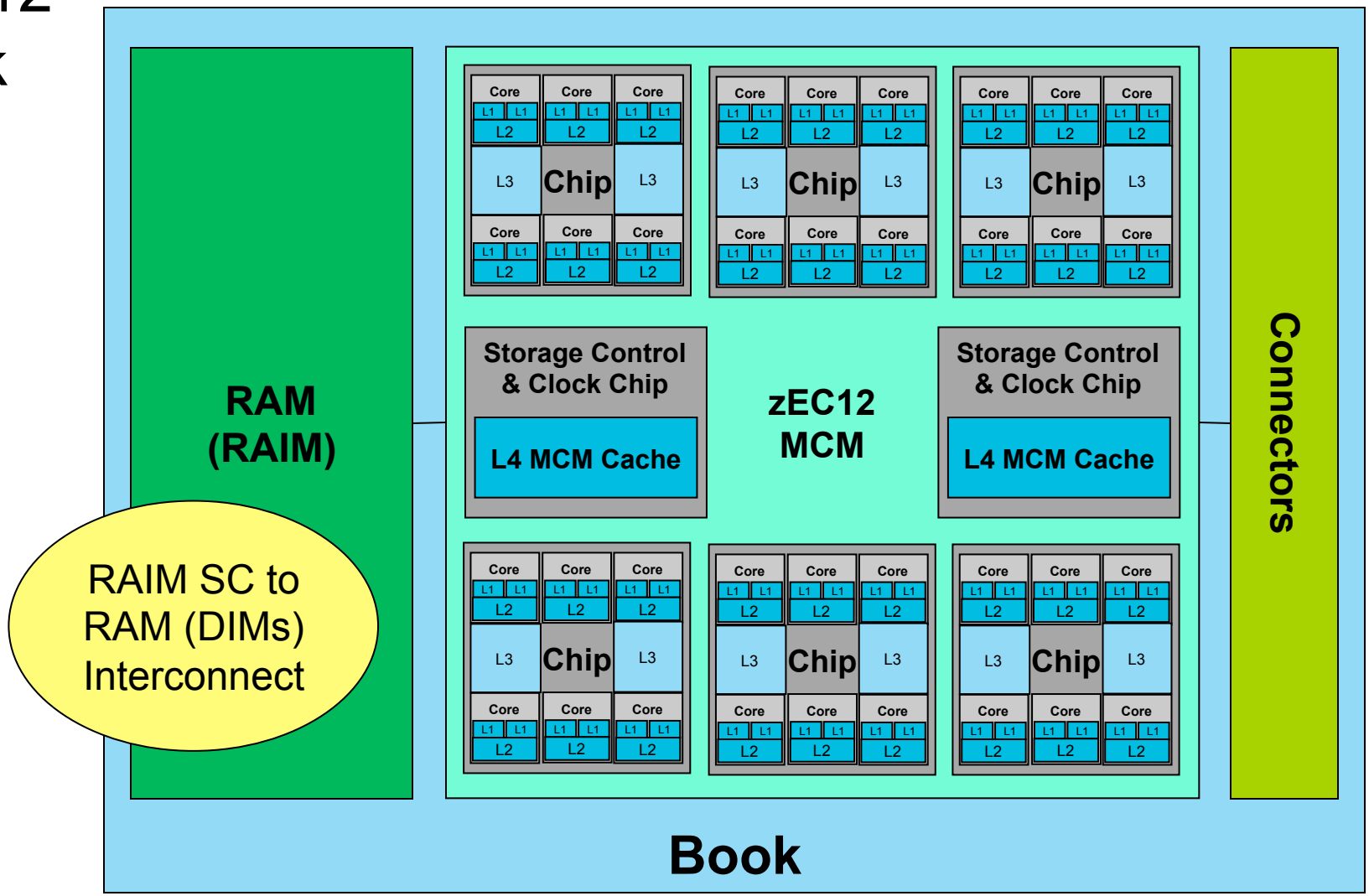
zEC12 Multi-Chip Module

L4 Shared 384MB

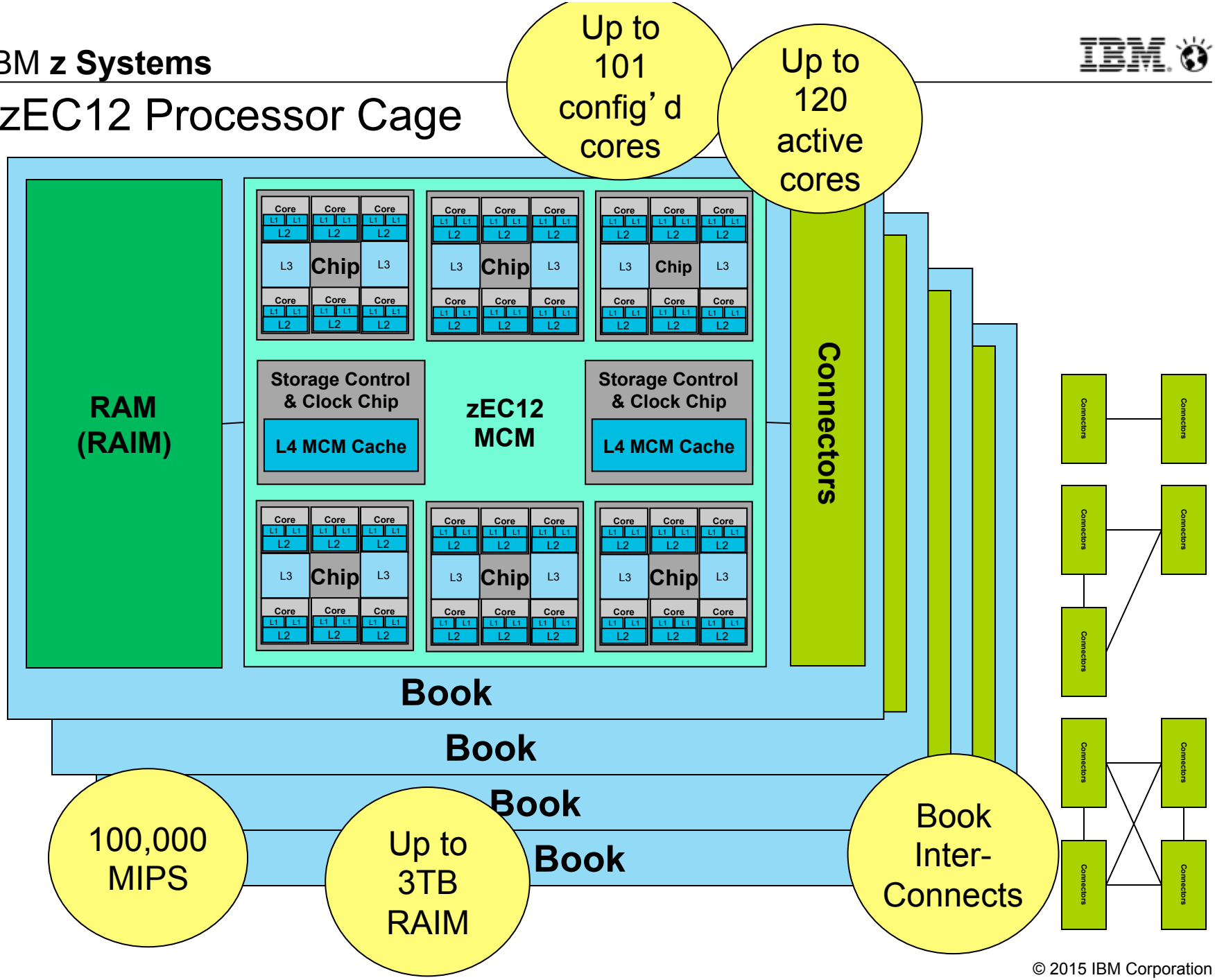
1800 Watts



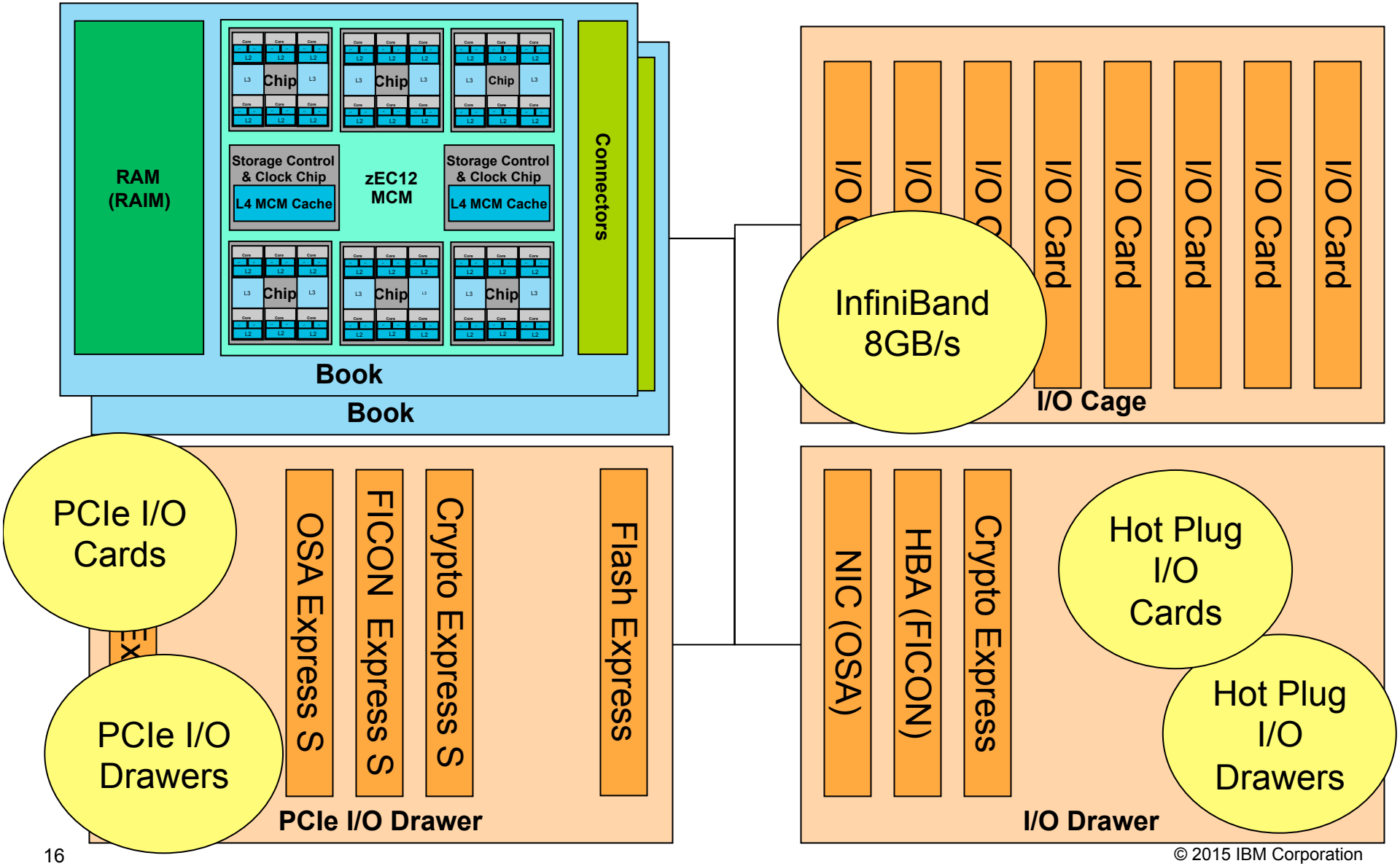
zEC12 Book



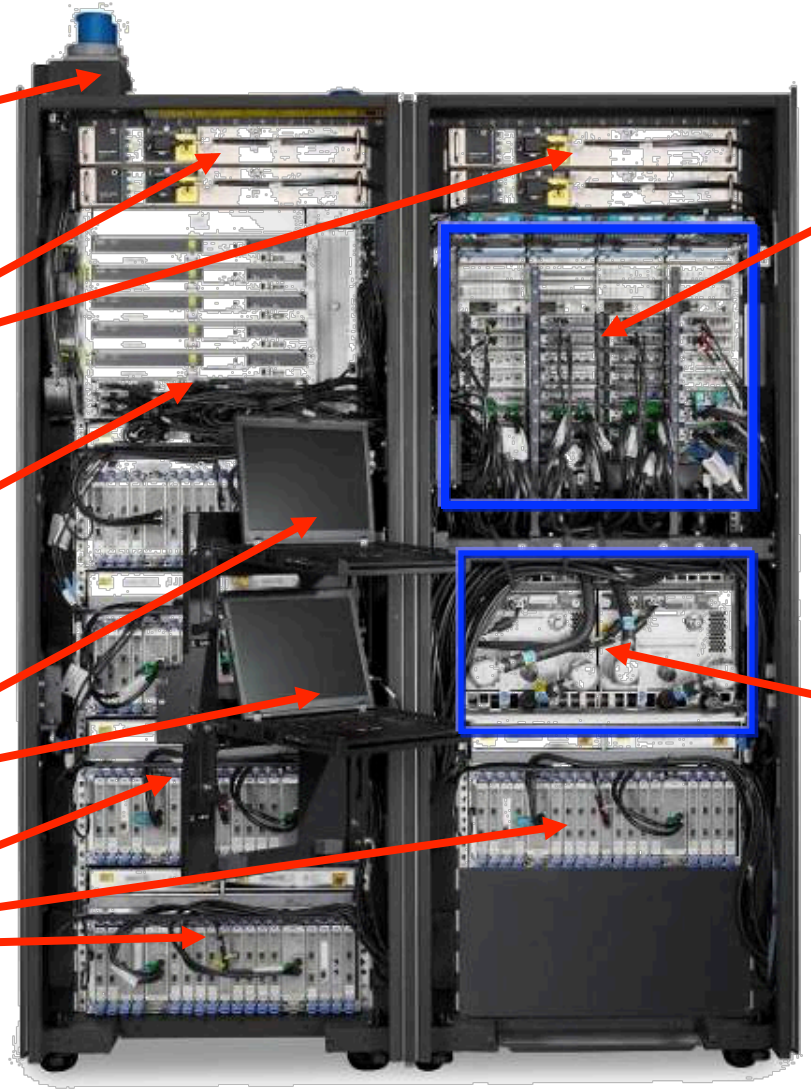
zEC12 Processor Cage



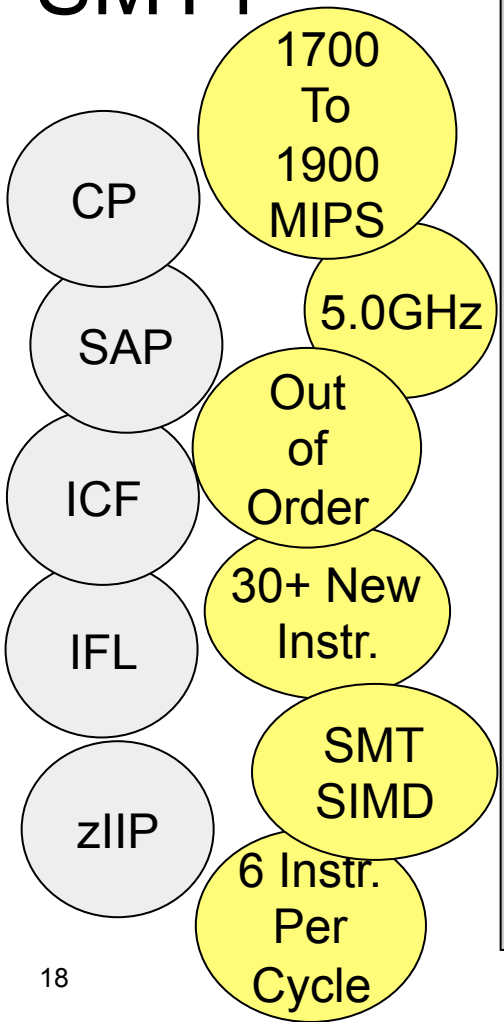
I/O Cages and Drawers

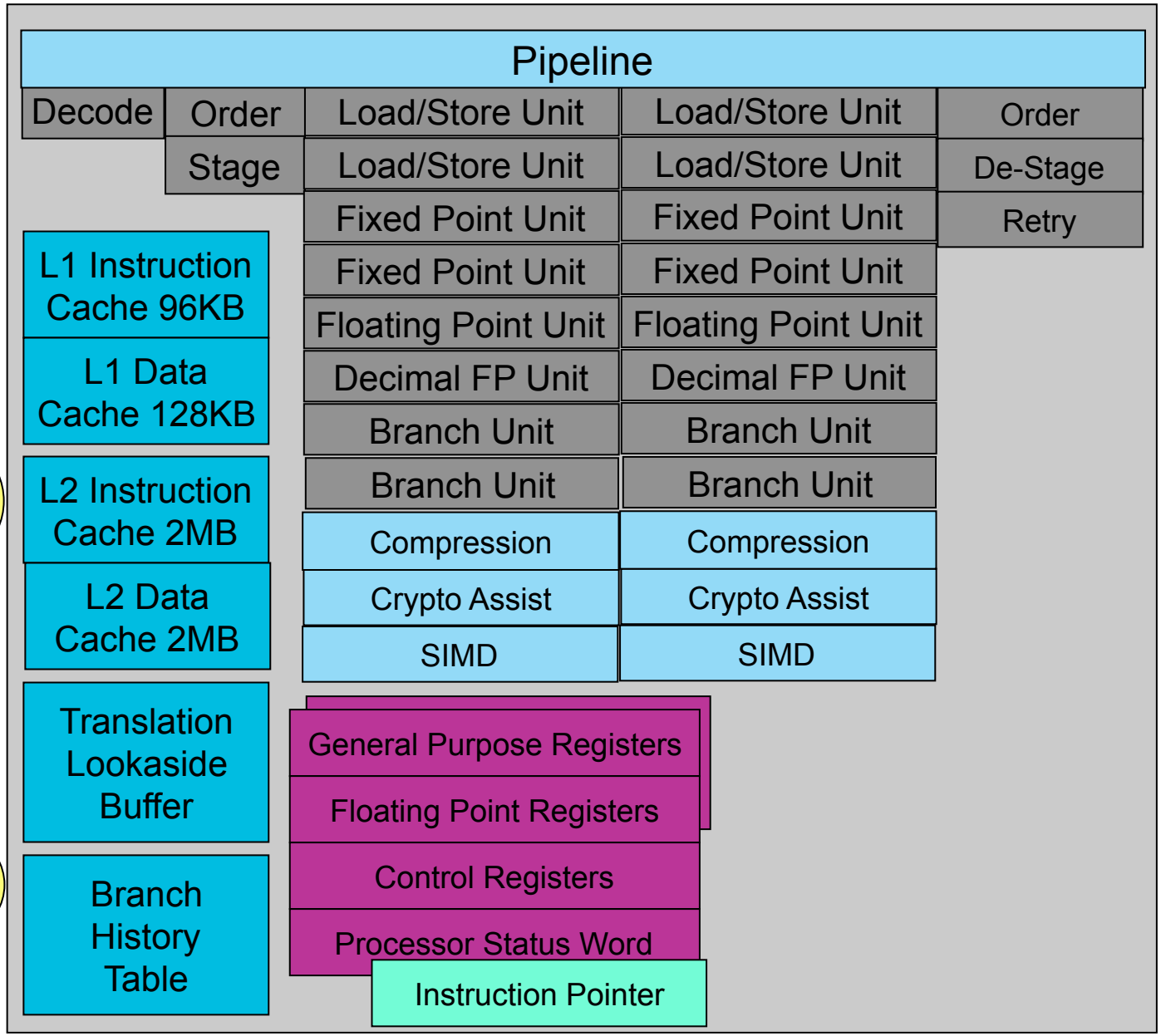


Under the zEC12 Covers

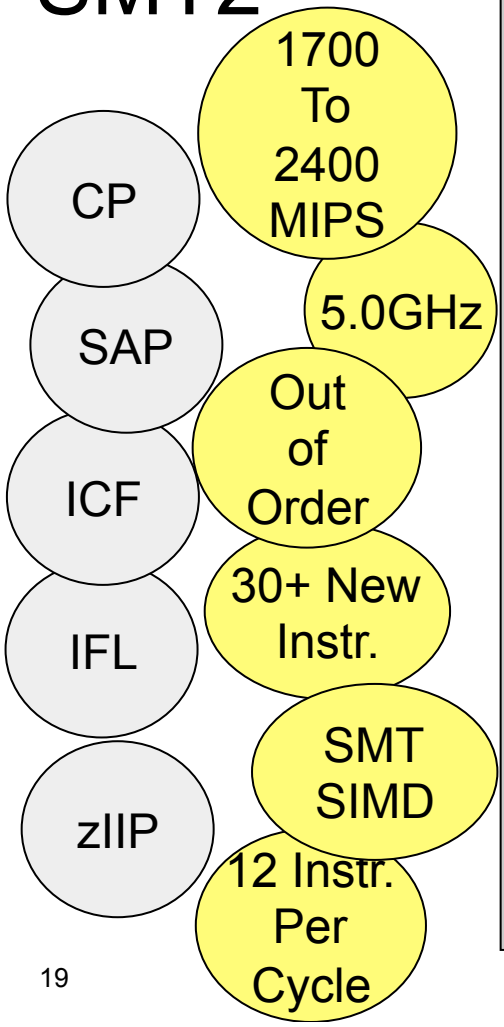


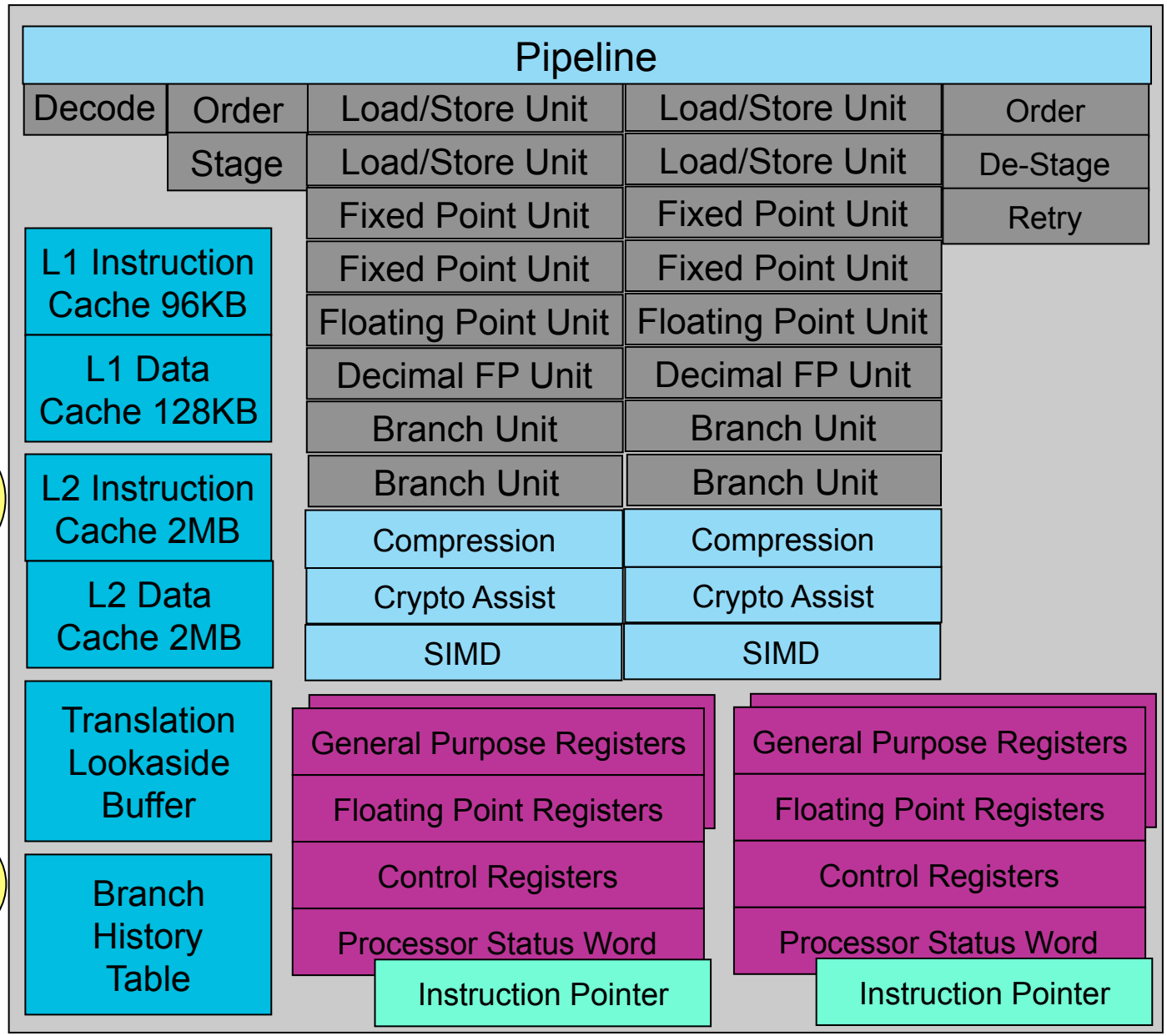
z13 Core SMT1





z13 Core SMT2



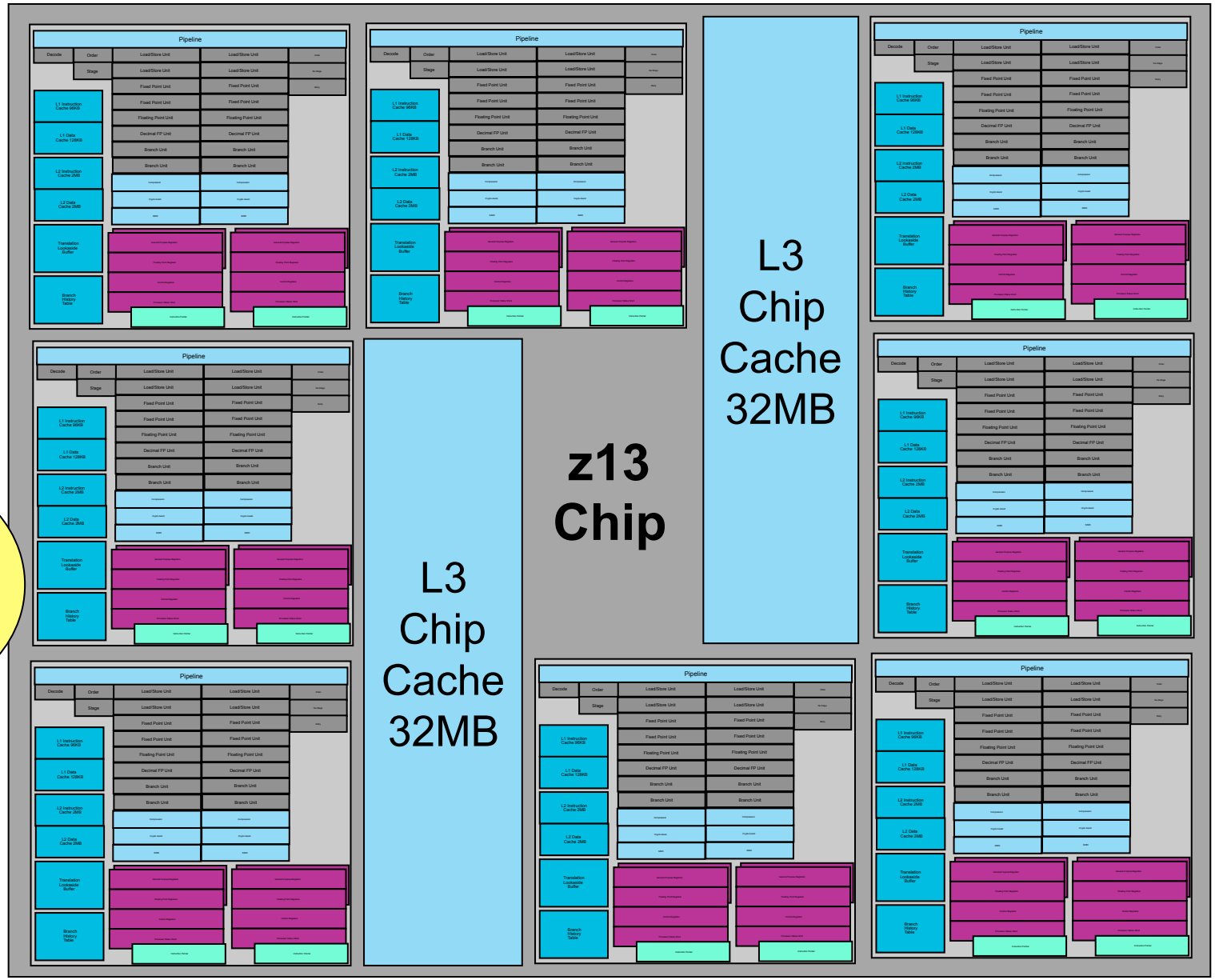


z13 Chip

3.99B Transistors

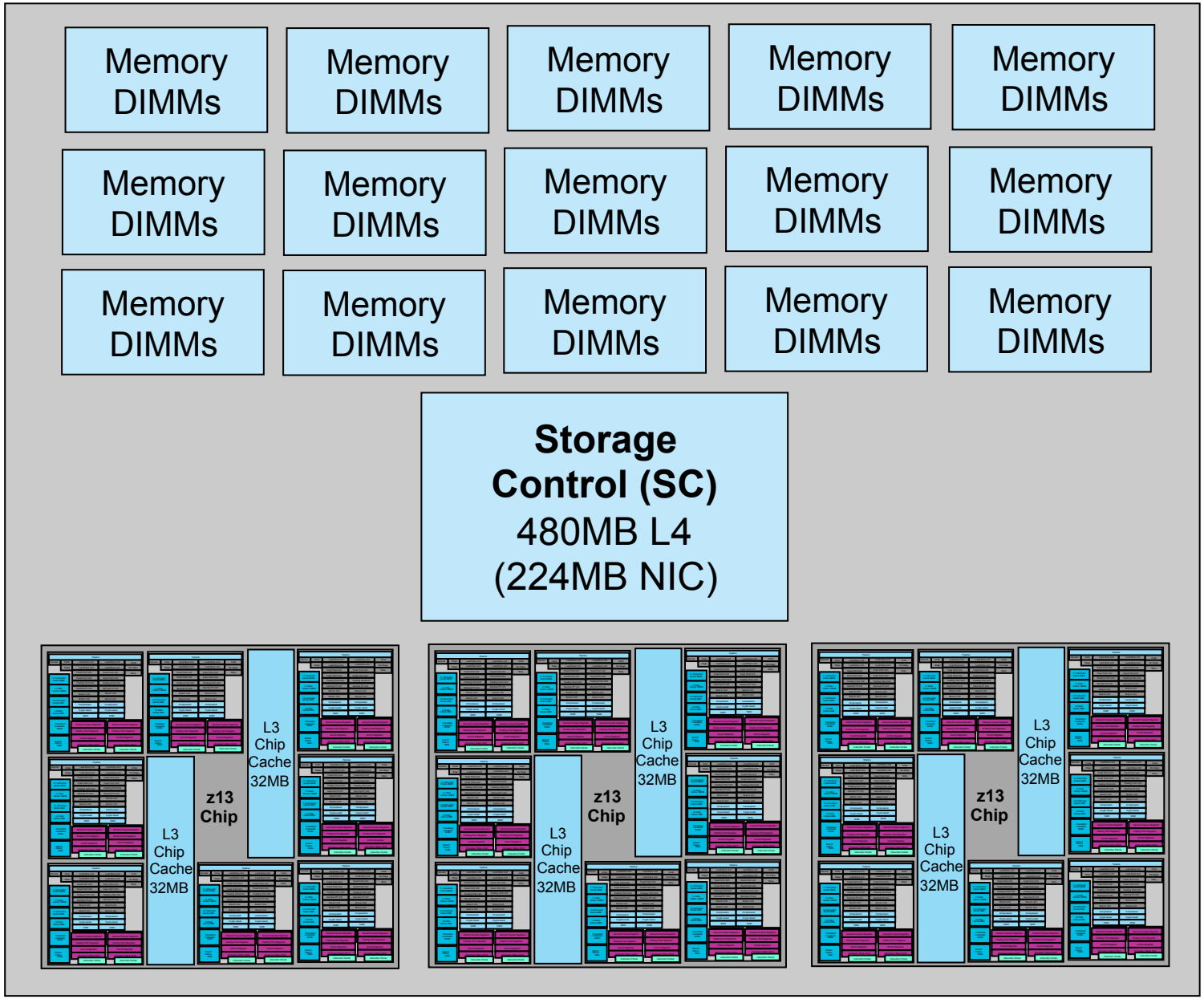
L1/L2/L3 Total 98MB cache

Oct-Core (max 8)



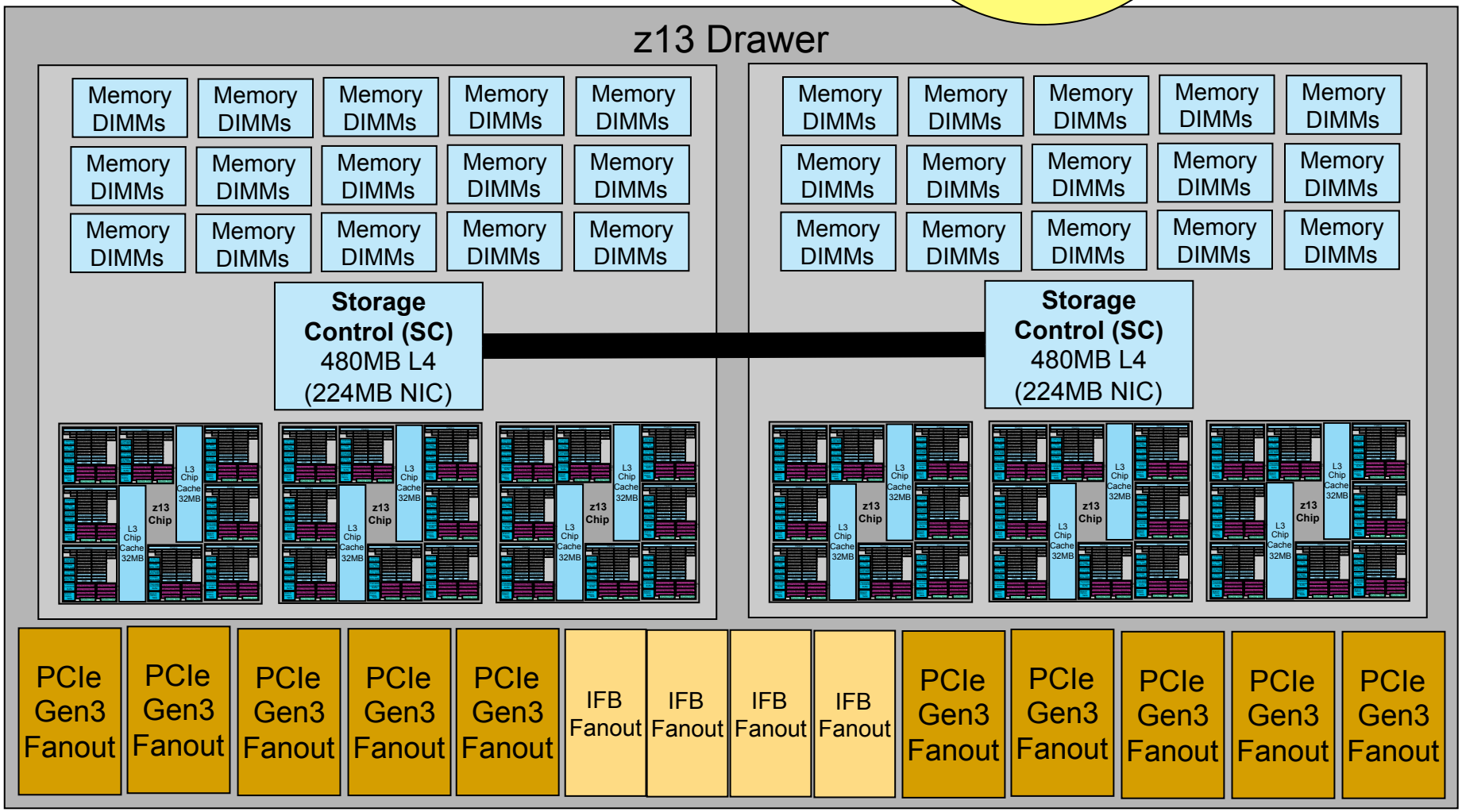
z13 Node

New Technology Packaging Domain

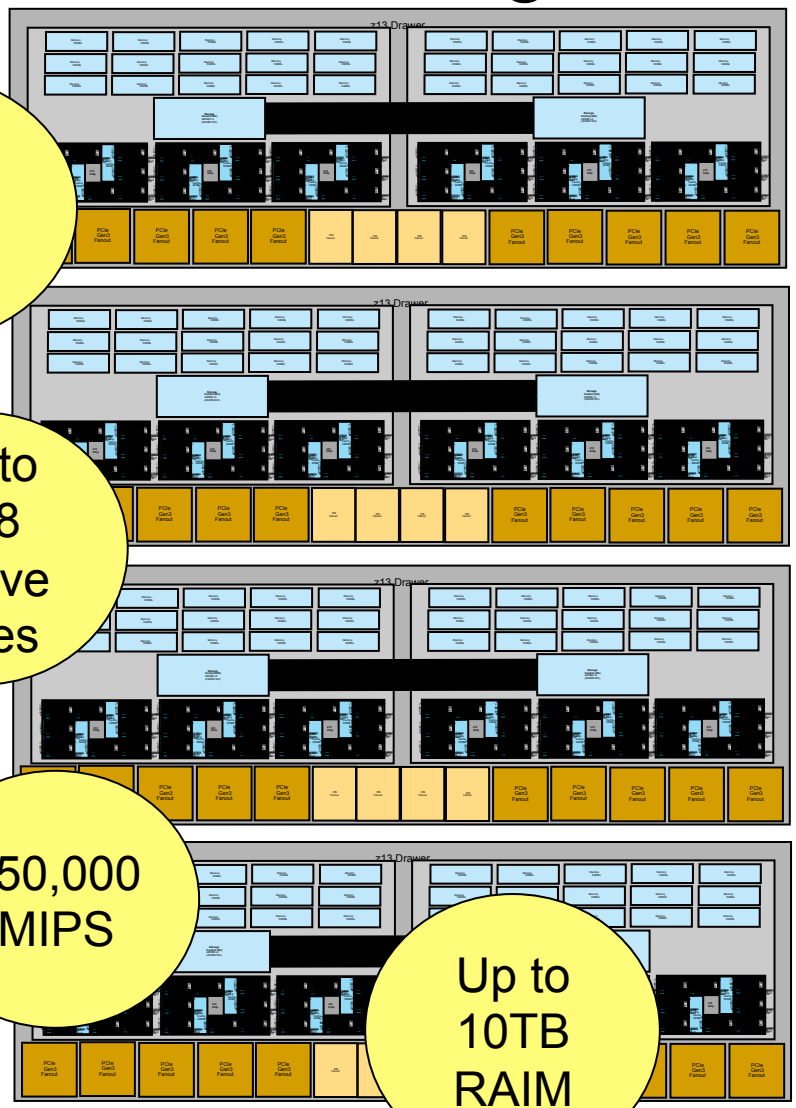


z13 Drawer

Akin to zEC12 MCM/Book



z13 Processor Cage



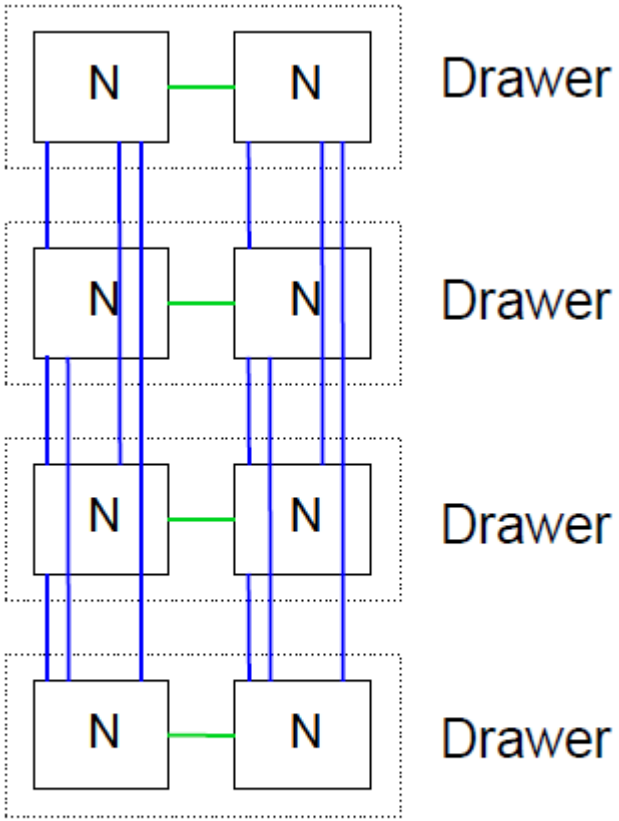
Up to 141 config'd cores

Up to 168 active cores

150,000 MIPS

Up to 10TB RAIM

Node and Drawer Interconnects



4 Drawer System Interconnect

z13 Processor Drawer to I/O Drawer

Max 5 PCIe Cages

PCIe Gen 3 16GB/sec Cage Interconnects

32 I/O Slots Per Cage

PCIe I/O Cards

PCIe I/O Drawers

Hot Plug Cages

Hot Plug Cards

PCIe I/O Drawer

OSA Express S

FICON Express S

Crypto Express S

Flash Express

PCIe I/O Drawer

Flash Express

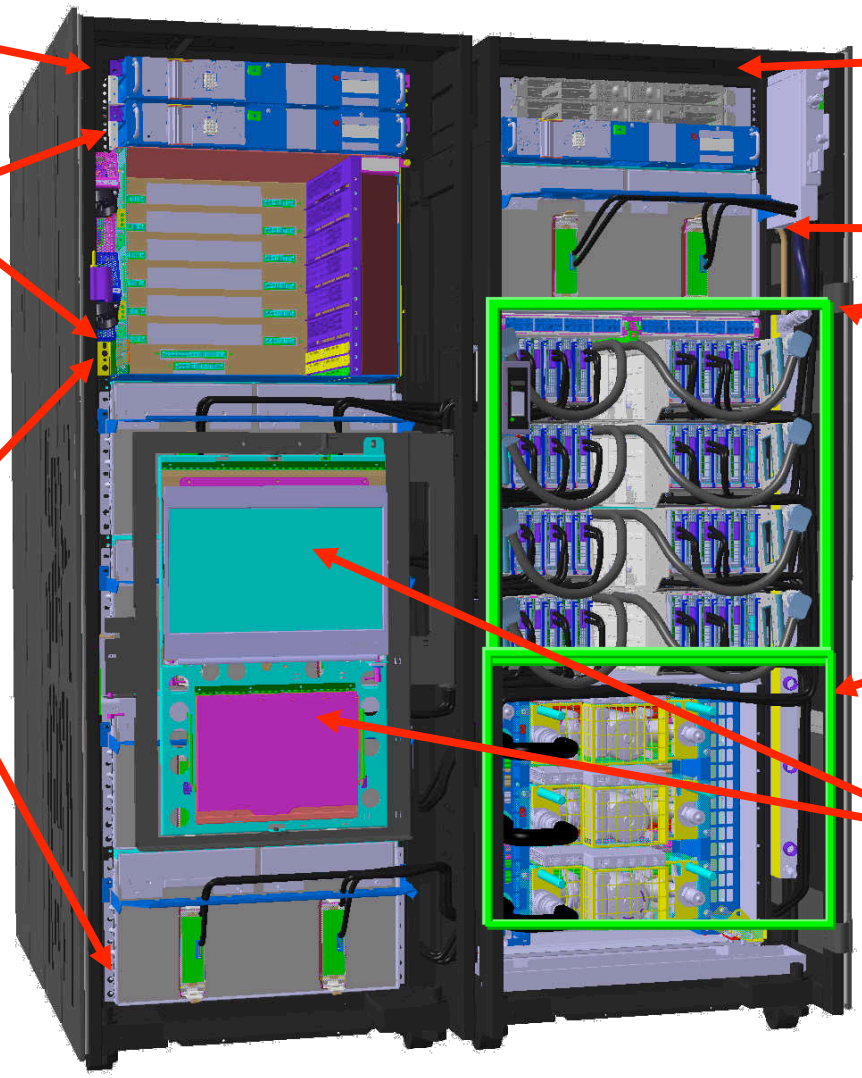
OSA Express S

FICON Express S

FICON Express S

FICON Expre

z13 Model NE1 or NC9 Radiator (Air) Cooled – Under the covers (Front View)



Optional Integrated Battery Features (IBFs)

Power Components

Space for the first four I/O drawers. The top two can be 8-slot for carried forward FICON Express8. All can be PCIe I/O drawers

Two 1U Support Element (SE) System Units

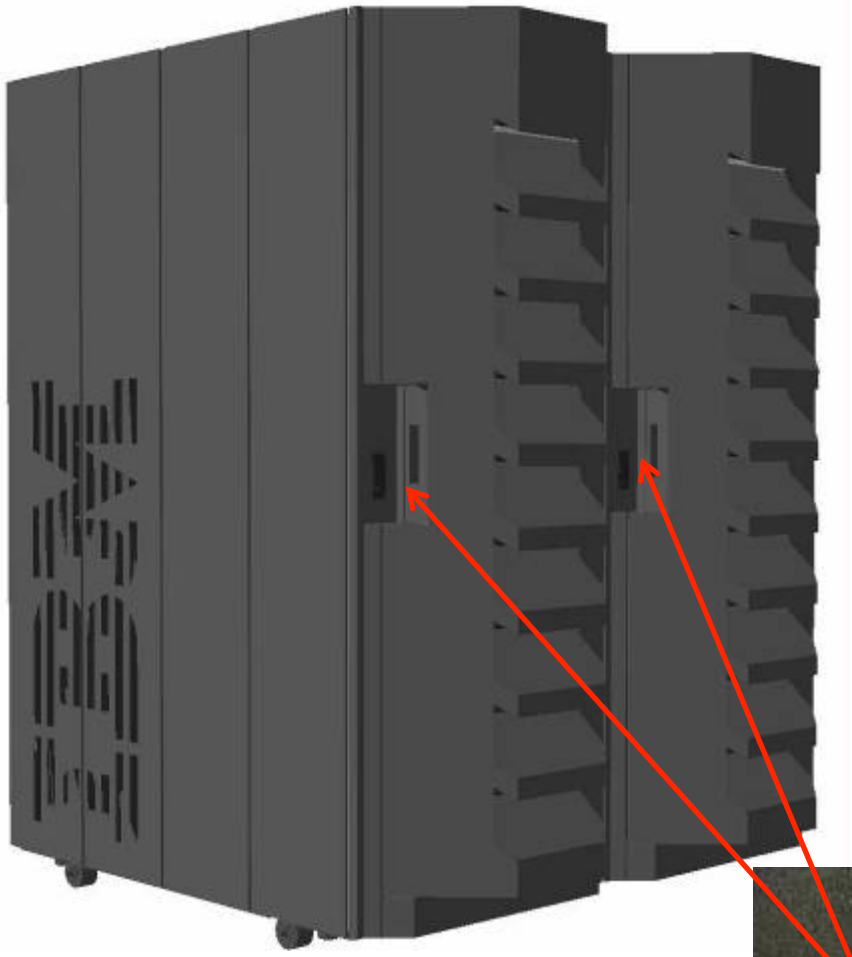
Space for the last PCIe I/O drawer

Processor Drawers (1st bottom to 4th top) with Flexible Support Processors (FSPs), and I/O fanouts

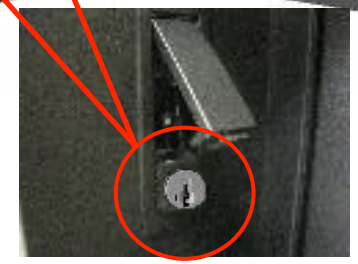
N+2 Pumps and Blowers for Radiator Air Cooling Unit

2 SE Displays with Keyboards

Z13 Door Design and Locks

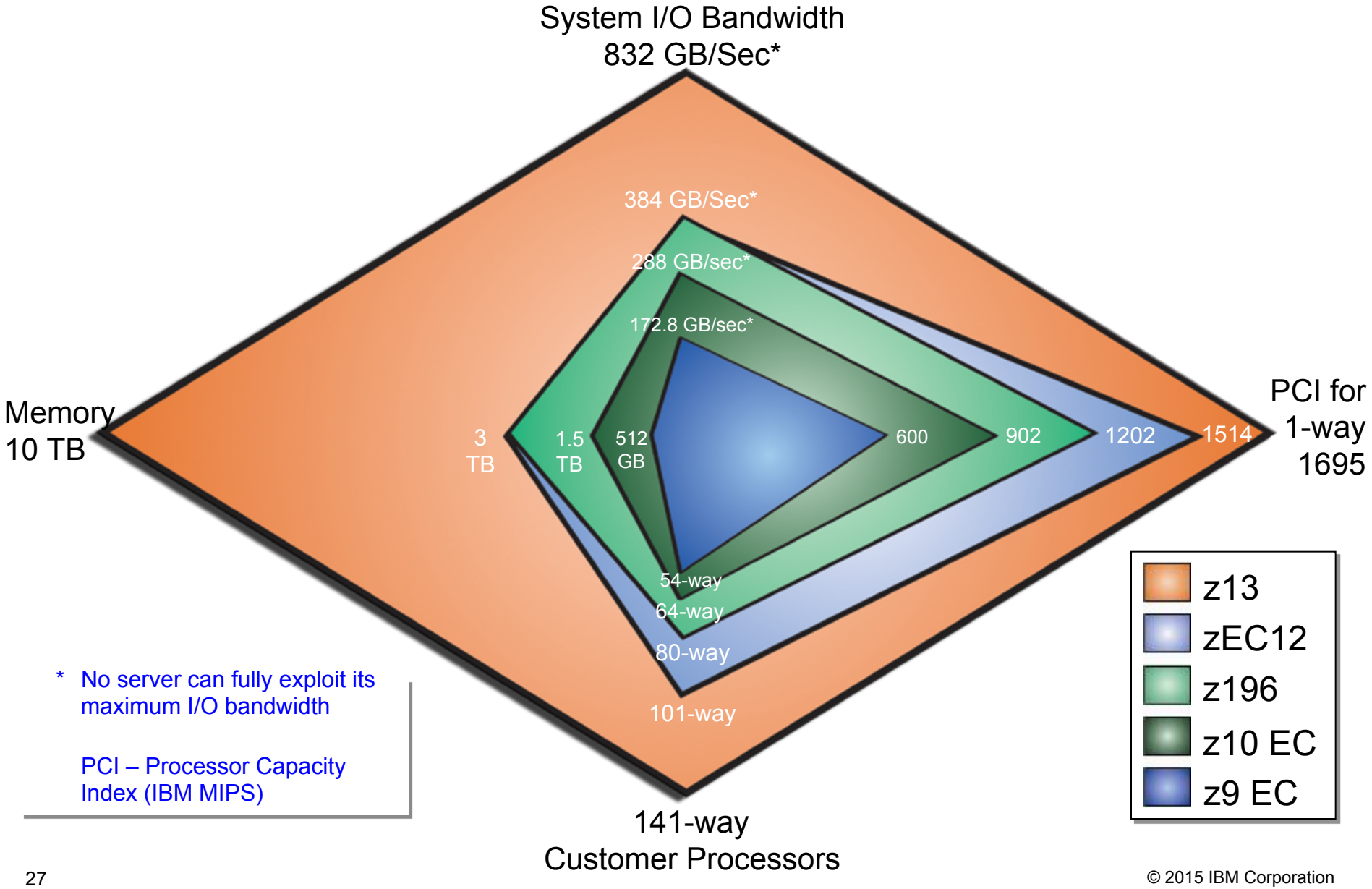


z13 System
Rear view
(vectored down oriented rear cover)



z13 System
Rear view
(vectored up oriented rear cover)

IBM z13: Advanced system design optimized for digital business



* No server can fully exploit its maximum I/O bandwidth

PCI – Processor Capacity Index (IBM MIPS)

z13 Processor Unit Allocation/Usage – zIIP to CP 2:1 ratio

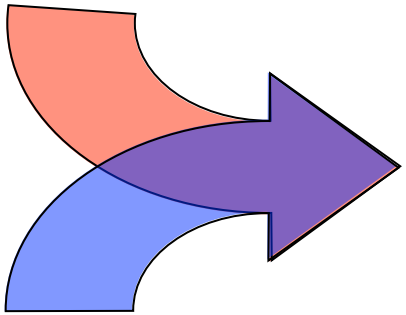
Model	Drawers /PUs	CPs	IFLs uIFLs	zIIPs	ICFs	Std SAPs	Optional SAPs	Std. Spares	IFP
N30	1/39	0-30	0-30 0-29	0-20	0-30	6	0-4	2	1
N63	2/78	0-63	0-63 0-62	0-42	0-63	12	0-8	2	1
N96	3/117	0-96	0-96 0-95	0-64	0-96	18	0-12	2	1
NC9	4/156	0-129	0-129 0-128	0-86	0-129	24	0-16	2	1
NE1	4/168	0-141	0-141 0-140	0-94	0-141	24	0-16	2	1

- z13 Models N30 to NC9 use drawers with 39 cores. The Model NE1 has 4 drawers with 42 cores.
- The maximum number of logical ICFs or logical CPs supported in a CF logical partition is 16
- The integrated firmware processor (IFP) is used for PCIe I/O support functions
- Concurrent Drawer Add is available to upgrade in steps from model N30 to model NC9

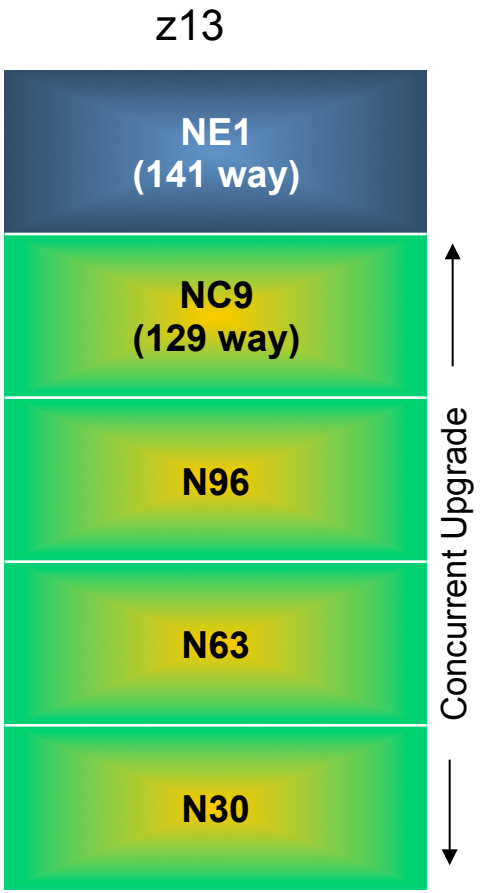
1. At least one CP, IFL, or ICF must be purchased in every machine
2. Two zIIPs may be purchased for each CP purchased if PUs are available. This remains true for sub-capacity CPs and for “banked” CPs.
3. On an upgrade from z196 or zEC12, installed zAAPs are converted to zIIPs by default. (Option: Convert to another engine type)
4. “uIFL” stands for Unassigned IFL
5. The IFP is conceptually an additional, special purpose SAP

z13 System Upgrades

zEC12 zBX Model 3



z196 zBX Model 2



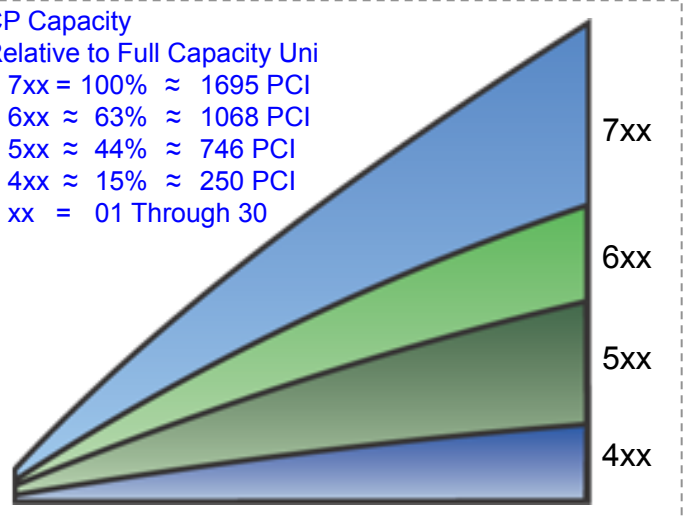
- z13 to z13 model upgrades
  - Upgrade of z13 Models N30, N63, N96 and NC9 to NE1 is disruptive
  - When upgrading to z13 Model NE1, all the CPC Drawers are replaced
  - Conversion* from Radiator-based air to Water cooled or Water to Radiator-based air cooling not available
- Any* z196 to any z13
- Any* zEC12 to any z13
  - Feature conversion of installed zAAPs to zIIPs (default) or another processor type
  - For installed On Demand Records, change temporary zAAPs to zIIPs. Stage the record
- When a z196 with a zBX Model 002 or zEC12 with a zBX Model 003 is upgraded to z13, the zBX is detached from the CPC and converted to a Model 004. The zBX becomes a Node without a CPC. Additional planning required and conditions apply

*Note:
Air to Water Conversions
- Conversions from z196 & zEC12 Air to z13 Water will be supported with a frame roll as was done on z196 & zEC12.
- Upgrading from a z13 Radiator based air to a z13 Water will only be offered via a Migration offering (8P2979). RPQ 8P2979 is ONLY available on initial orders and not available as an MES.

Water to Air conversions
- Conversions from water to air are NOT supported for either z196, zEC12 or z13 to z13.

z13 Full and Sub-Capacity CP Offerings

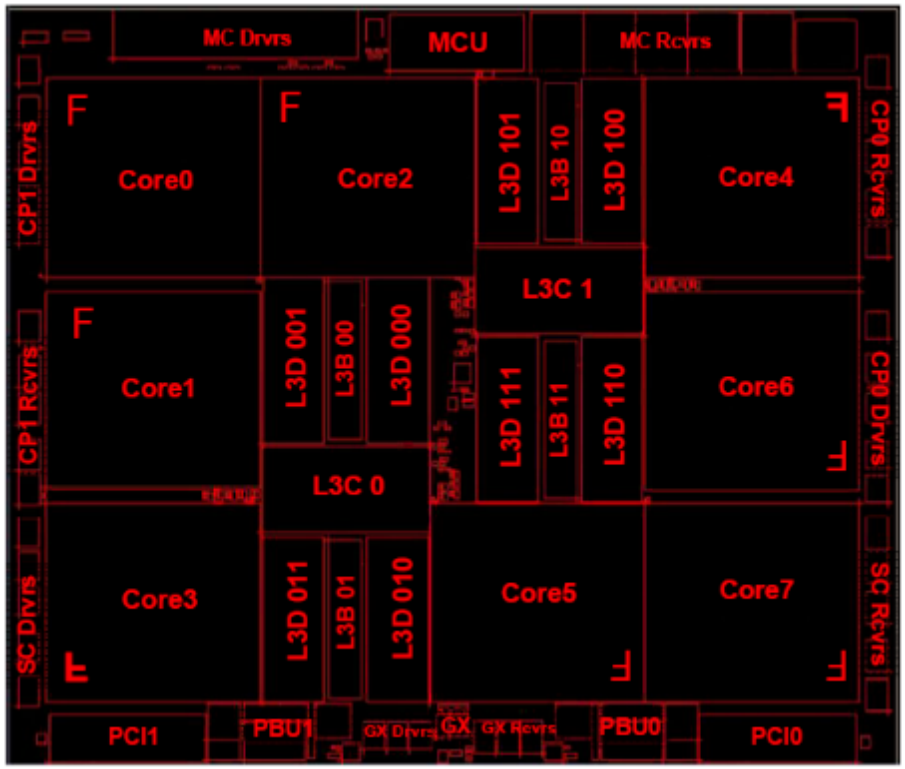
CP Capacity
Relative to Full Capacity Uni
7xx = 100% ≈ 1695 PCI
6xx ≈ 63% ≈ 1068 PCI
5xx ≈ 44% ≈ 746 PCI
4xx ≈ 15% ≈ 250 PCI
xx = 01 Through 30



- Subcapacity CPs, up to 30, may be ordered on ANY z13 model. If 31 or more CPs are ordered all must be full 7xx capacity
- All CPs on a z13 CPC must be the same capacity
- All specialty engines are full capacity.
- zIIP to CP ratio – 2:1 and is the same for CPs of any capacity. No zAAPs available on z13
- Only 30 CPs can have granular capacity but other PU cores may be characterized as full capacity specialty engines
- For no CPs, the capacity setting is 400
- Total of 231 Capacity settings
- PVU for z13 is 120

MSU Sub Capacity

z13 8-Core Processor Unit (PU) Chip Detail

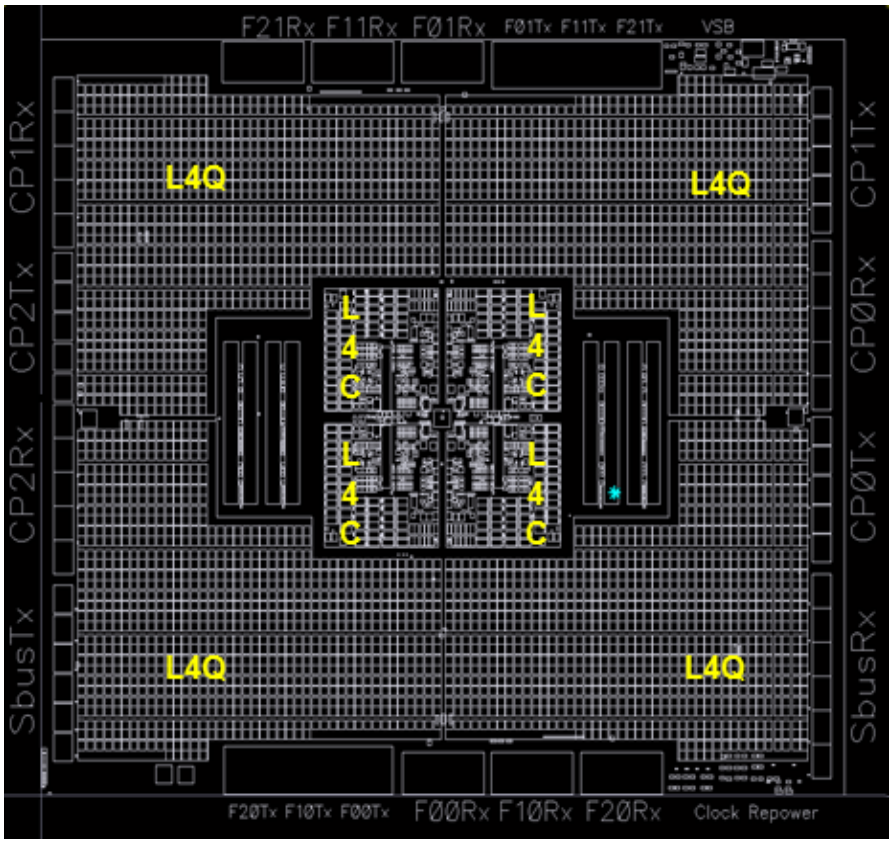


- 14S0 22nm SOI Technology
  - 17 layers of metal
  - 3.99 Billion Transistors
  - 13.7 miles of copper wire
- Chip Area
  - 678.8 mm^2
  - 28.4 x 23.9 mm
  - 17,773 power pins
  - 1,603 signal I/Os

- Up to eight active cores (PUs) per chip
  - 5.0 GHz (v5.5 GHz zEC12)
  - L1 cache/ core
    - 96 KB I-cache
    - 128 KB D-cache
  - L2 cache/ core
    - 2M+2M Byte eDRAM split private L2 cache
- Single Instruction/Multiple Data (SIMD)
- Single thread or 2-way simultaneous multithreading (SMT) operation
- Improved instruction execution bandwidth:
  - Greatly improved branch prediction and instruction fetch to support SMT
  - Instruction decode, dispatch, complete increased to 6 instructions per cycle
  - Issue up to 10 instructions per cycle
  - Integer and floating point execution units
- On chip 64 MB eDRAM L3 Cache
  - Shared by all cores
- I/O buses
  - One InfiniBand I/O bus
  - Two PCIe I/O buses
- Memory Controller (MCU)
  - Interface to controller on memory DIMMs
  - Supports RAIM design

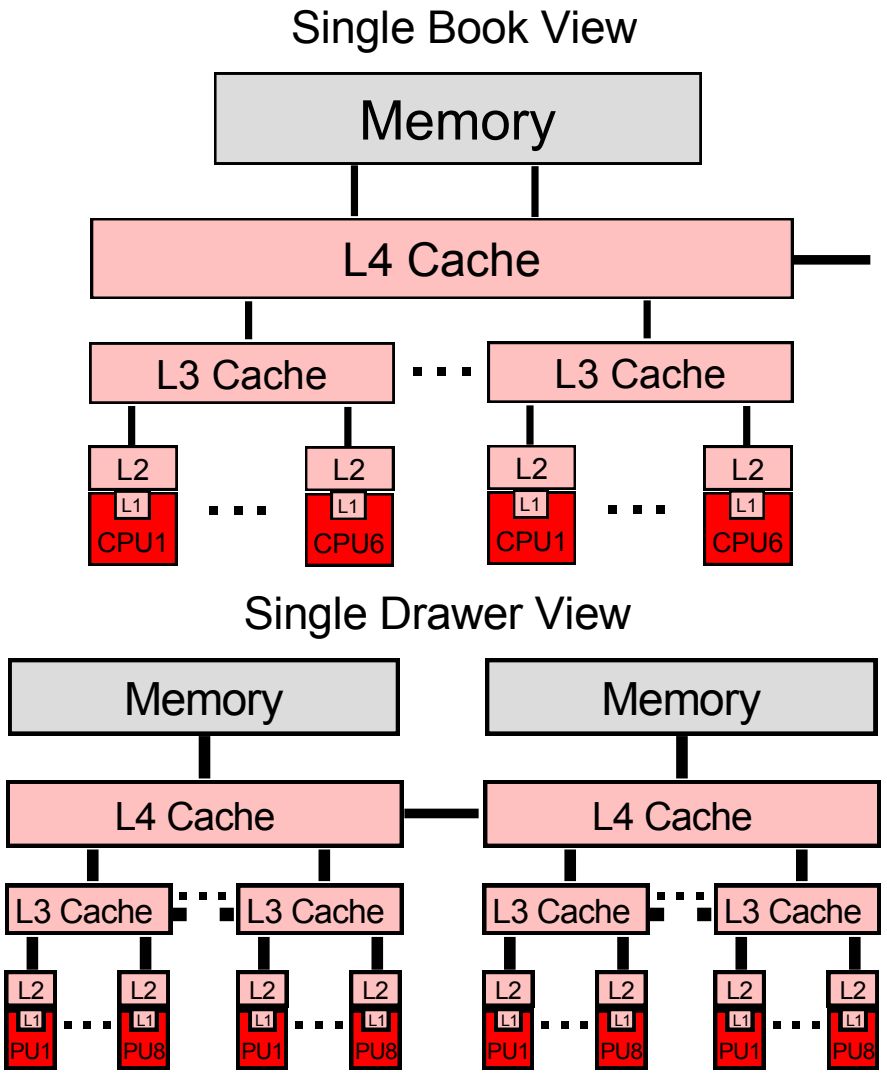
z13 Storage Control (SC) Chip Detail

- **CMOS 14S0 22nm SOI Technology**
  - 15 Layers of metal
  - 7.1 Billion transistors
  - 12.4 Miles of copper wire
- **Chip Area** –
  - 28.4 x 23.9 mm
  - 678 mm²
  - 11,950 power pins
  - 1,707 Signal Connectors
- **eDRAM Shared L4 Cache**
  - 480 MB per SC chip (Non-inclusive)
  - L3 NIC Directory
  - 2 SCs = 960 MB L4 per z13 drawer
- **Interconnects (L4 – L4)**
  - **3 to CPs in node**
  - **1 to SC (node – node) in drawer**
  - **3 to SC nodes in remote drawers**
- **6 Clock domains**



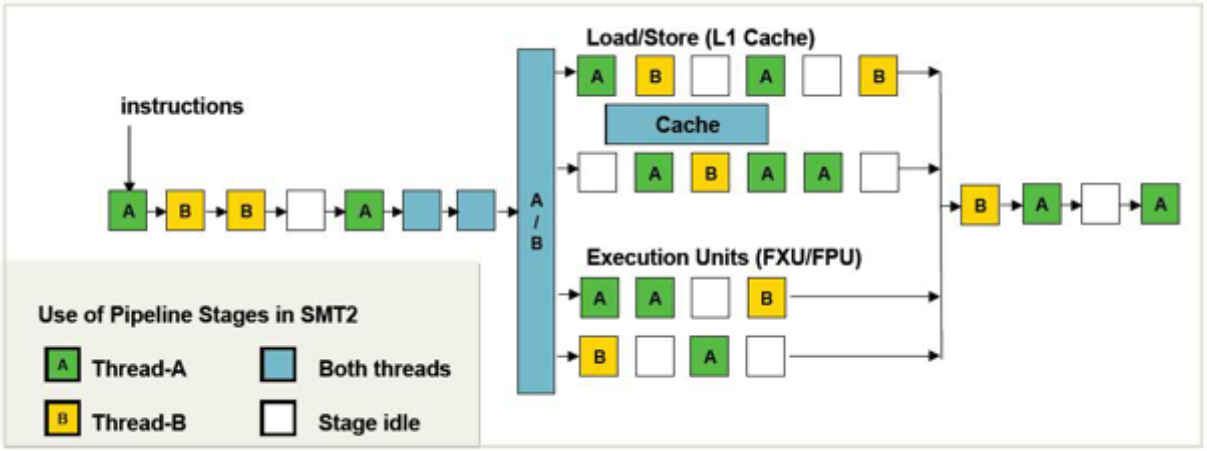
z13 versus zEC12 Hardware Comparison

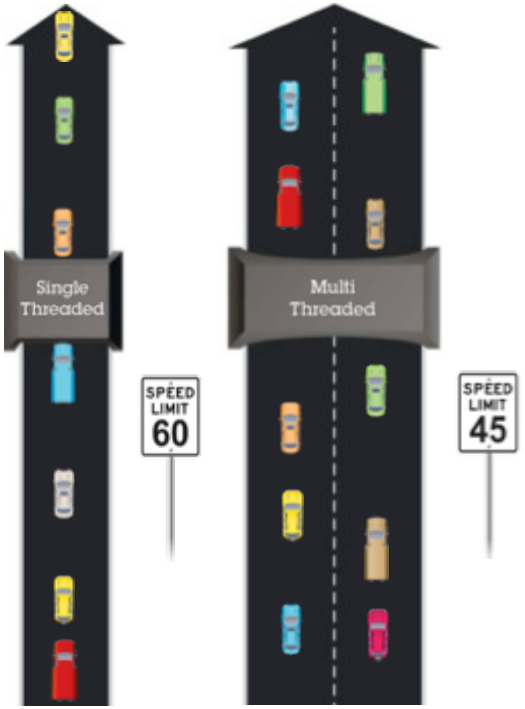
- **zEC12**
  - CPU
    - 5.5 GHz (1514 PCI)
    - Enhanced Out-Of-Order
  - Caches
    - L1 private 64k i, 96k d
    - L2 private 1 MB i + 1 MB d
    - L3 shared 48 MB / chip
    - L4 shared 384 MB / book
- **z13**
  - CPU
    - 5.0 GHz (1695 PCI)
    - Major pipeline enhancements
  - Caches
    - L1 private 96k i, 128k d
    - L2 private 2 MB i + 2 MB d
    - L3 shared 64 MB / chip
    - L4 shared 960 MB / drawer
      - plus 448 MB NIC



IBM z13: SMT – Simultaneous Multi-Threading

- Double the number of hardware threads per core
  - Independent threads can be more effective utilizing pipeline
- Threads share resources – may impact single thread perf
  - Pipeline (eg. physical registers, fxu, fpu, lsu etc)
  - Cache
- Throughput improvement is workload dependent



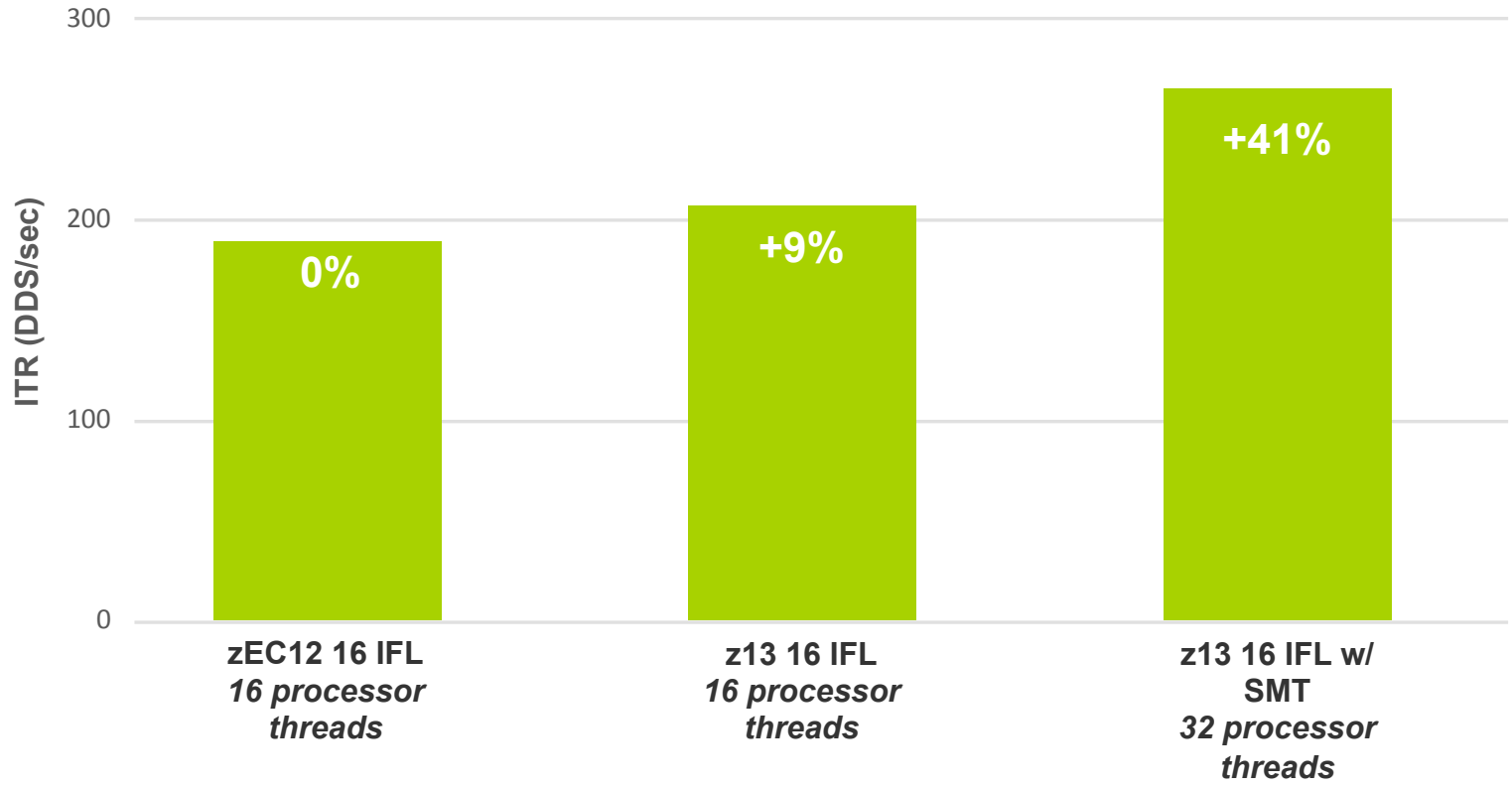


Two zIIP lanes handle more traffic overall

z13 – SAP AppServer IFL capacity with SMT

SAP Application Server is a good candidate for SMT
Lots of concurrent threads.

SAP AppServer on Linux under z/VM

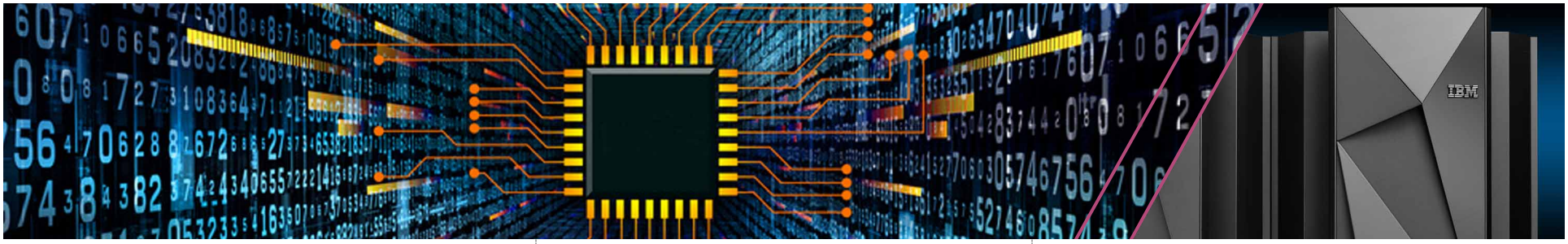


(Controlled measurement environment, results may vary)

 http://www.redbooks.ibm.com/abstracts/redp5144.html?Open

Specialty engines expand the use of the mainframe

While lowering the cost of ownership



zIIP*

- ***Relieves*** central processors of running specific workloads
- Optimized for strategic web based applications with support for ***Java and XML*** processing
- Focused on data and supporting workloads can help ***connect, manage, extend, and protect*** data

IFLs and Enterprise Linux Server

- Special engine dedicated to ***Linux workloads*** on z Systems servers
- ***IT optimization and cloud computing*** can deliver enhanced economics
- Attractively priced and supported by the z/VM virtualization, the IBM Wave virtualization management and the Linux operating system

Coupling Facility

- CF allows multiple processors to access the same data
- New with z13 is support for 256 CHPIDs (2X available on zEC12)
- ***New PCIe*** based short range coupling links

zIIP and IFLs get throughput increase with simultaneous multithreading

IBM

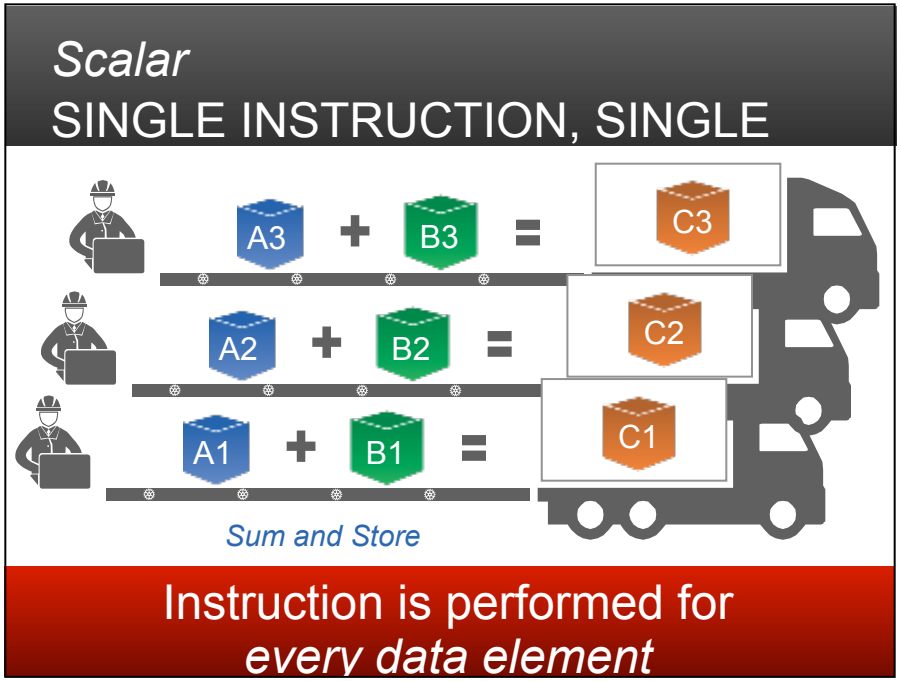
* Supports 2:1 ratio for zIIP to CP

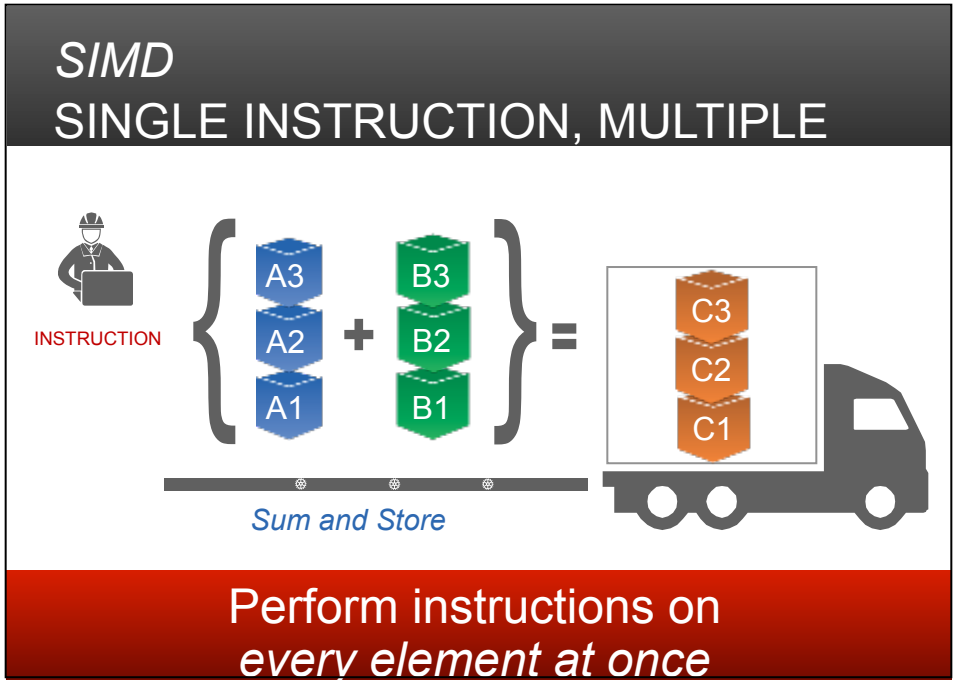
SIMD (Single Instruction Multiple Data) processing

Increased parallelism to enable analytics processing

- Smaller amount of code helps improve execution efficiency
- Process elements in parallel enabling more iterations
- Supports analytics, compression, cryptography, video/ imaging processing

Value
- ✓ Enable new applications
- ✓ Offload CPU
- ✓ Simplify coding





Java, Compilers, Odds and Ends

SIMD **Transparent Execution Mode** allows workloads from previous generation systems to run directly on the z13 and gain SIMD acceleration benefits without explicit programming of the SIMD accelerator.

- **JAVA 8 Primitives** – Primitive operations are between 1.6x and 60x faster.
- **JAVA 8 CPU Intensive Benchmark -** Shows a composite improvement of 61% over zEC12 and Java7 SR4.
- **Business Rules Processing** - Shows an aggregate 2.27x improvement from IBM Java 8 and IBM z13

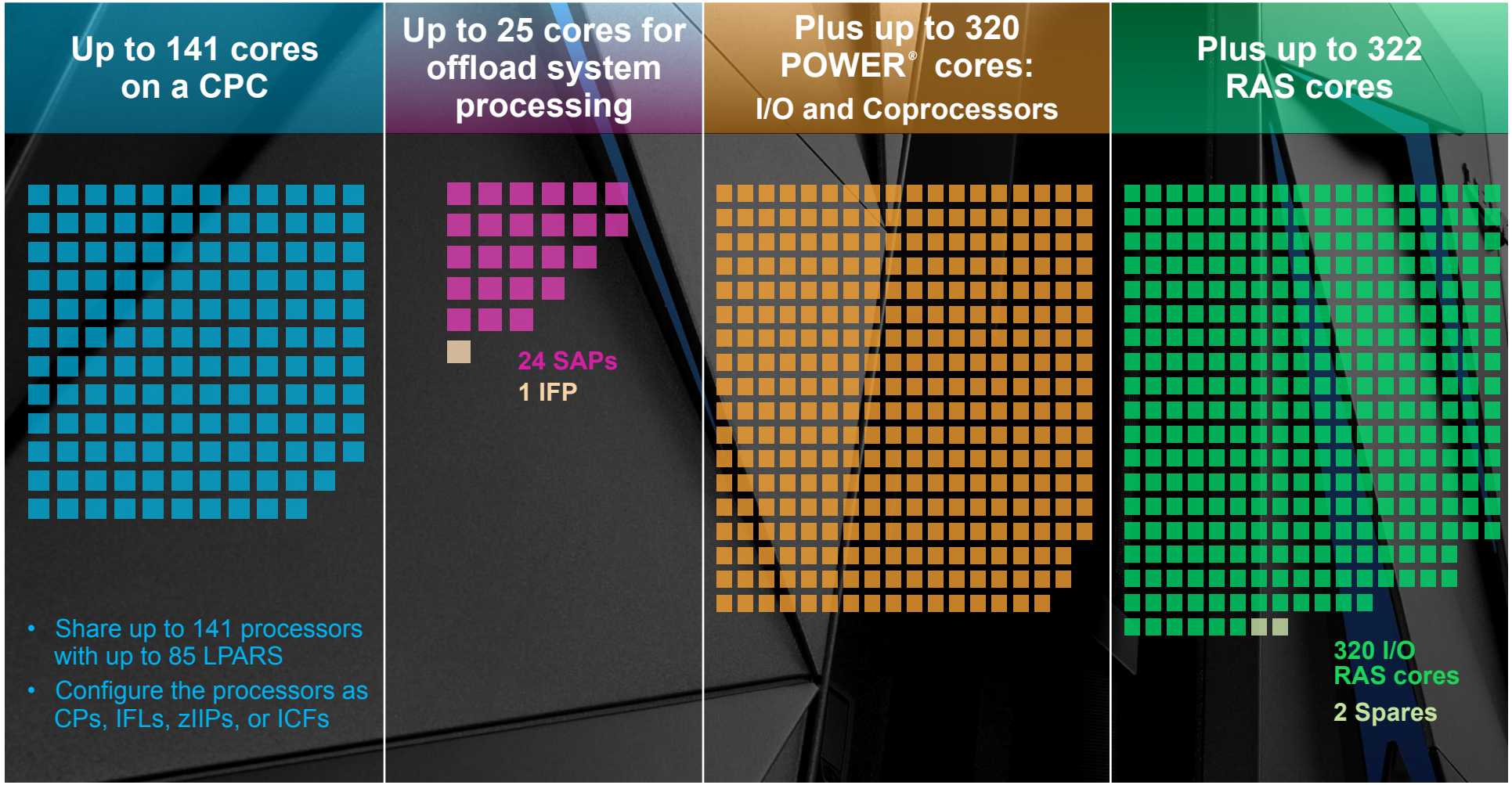
SIMD **Transformational Execution Mode** supports workloads that are enabled for SIMD acceleration by installing the upgraded IBM Compiler and Language Environment.

- **Enterprise COBOL for z/OS 5.2** – Planned GA 2.27, 14% reduction in CPU time for computationally intensive batch.
- **Enterprise PL/I 4.5** – Planned GA 2.27, 17% reduction in CPU time.

The high performance mathematics libraries (MASS, ATLAS) are available for the first time on z/OS and Linux on z (for C/C++ Usage).

Integrated system design

I/O and coprocessors bring RAS, cost savings and added compute power to workloads

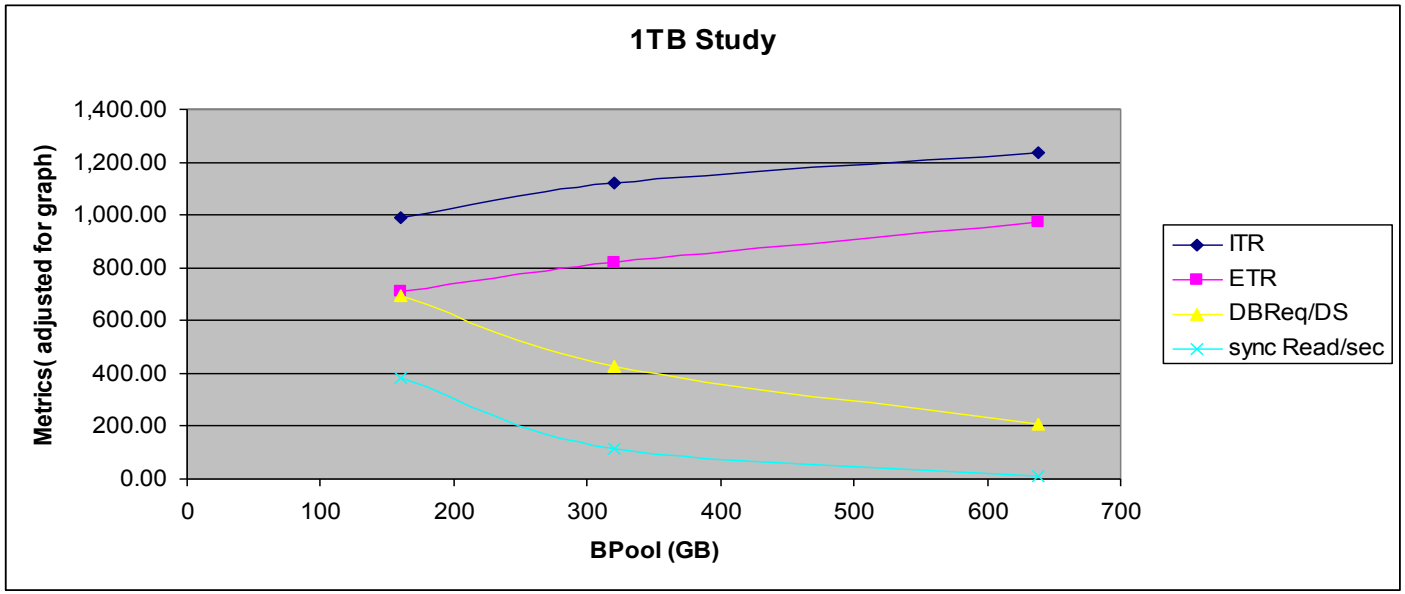


More memory makes a difference

- Up to 10 TB available memory
- Transparently support shrinking batch windows and meet service goals – ***no change to applications*** needed to gain benefits
- Get more work done – online transaction processing can experience ***up to 70% reduction in response time*** with more memory
- Improve system performance, ***minimize constraints and simplify management of applications*** with database middleware exploitation of additional memory
- Adding additional memory can increase sales and client satisfaction when you ***cut response time in half***
- ***Achieve faster decision making*** with the advantages of in memory data
- Improves real to virtual ratio that allows deployment and support for ***more Linux*** workloads

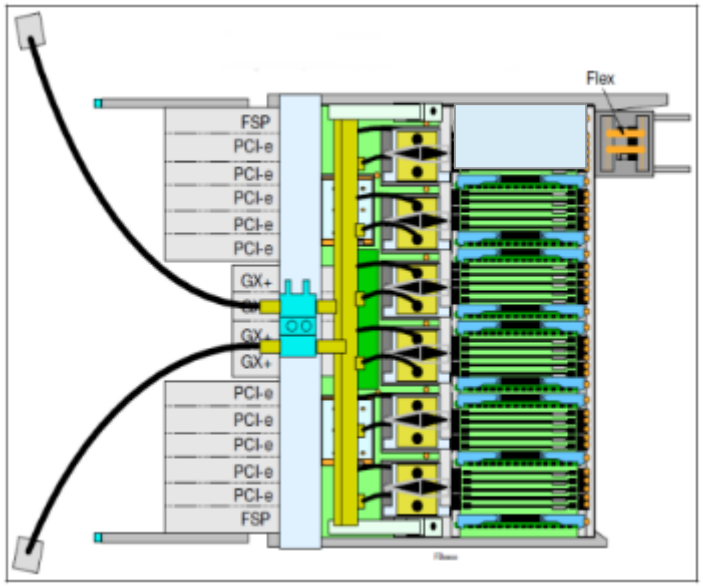
SSI: Online banking workload 12w DB2 V11 z/OS1.13

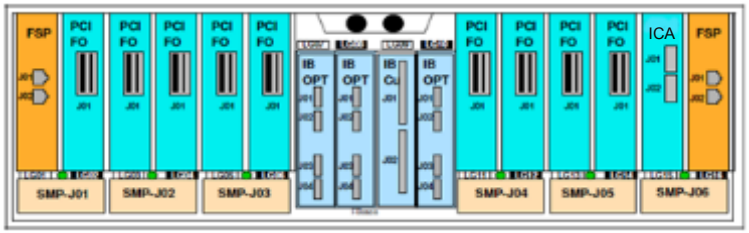
Memory♪	BP Size ♪	CPU %♪	ITR♪	ITR Delta♪	ETR♪	ETR Delta♪	Txn response time(sec)♪	Response time delta♪	Sync Read IO/sec♪	Sync IO delta♪
256 GB♪	160 GB♪	72♪	992♪	n/a♪	709♪	n/a♪	.695♪	n/a♪	38.4k♪	n/a♪
512 GB♪	320 GB♪	73♪	1124♪	13.3%♪	819♪	15.5%♪	.428♪	-38%♪	11.7k♪	-69%♪
1024 GB♪	638 GB♪	79♪	1237♪	24.7%♪	976♪	37.7%♪ ♪	.209♪	-70%♪	0.9k♪	-97%♪



CPC Drawer RAS Enhancements

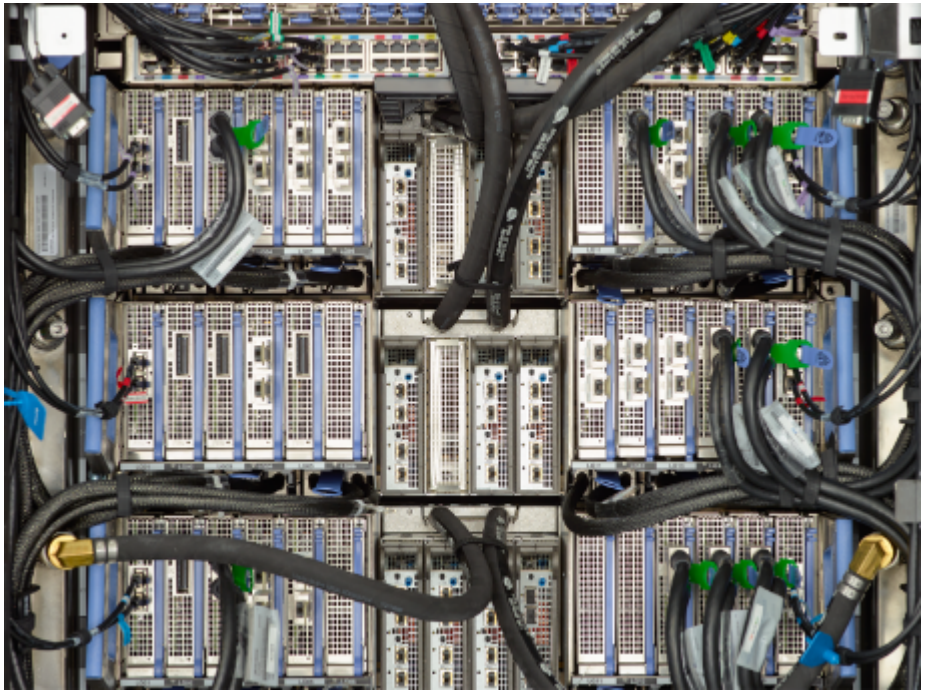
- z13 uses CPC drawers
  - Used in the BC z Systems
- PU and SC are SCMs, are field replaceable units (FRUs)
- POL (point of load) replaces Voltage Transformation Module (VTM)
  - now a FRU
- Water manifold is a FRU
- Redundant Oscillators isolated on their own backplane
- PU SCM is a FRU with universal spare
- SC SCM is a FRU
- CPC Drawer is a FRU (empty)
- CPC Drawer level degrade (1/2 drawer on single drawer)





Connecting the CPC Drawers

- The new drawer structure introduces cables between the drawers
  - Keyed cables to ensure correct length is plugged
  - Plugged detect to correct location
  - Custom latch to ensure retention



- Built in Time Domain Reflectometry (TDR) to isolate failures on
  - SMP cables (between drawer)
  - Between Chips (CP-CP, CP-SC, SC-SC)
  - Between CP and memory DIMM

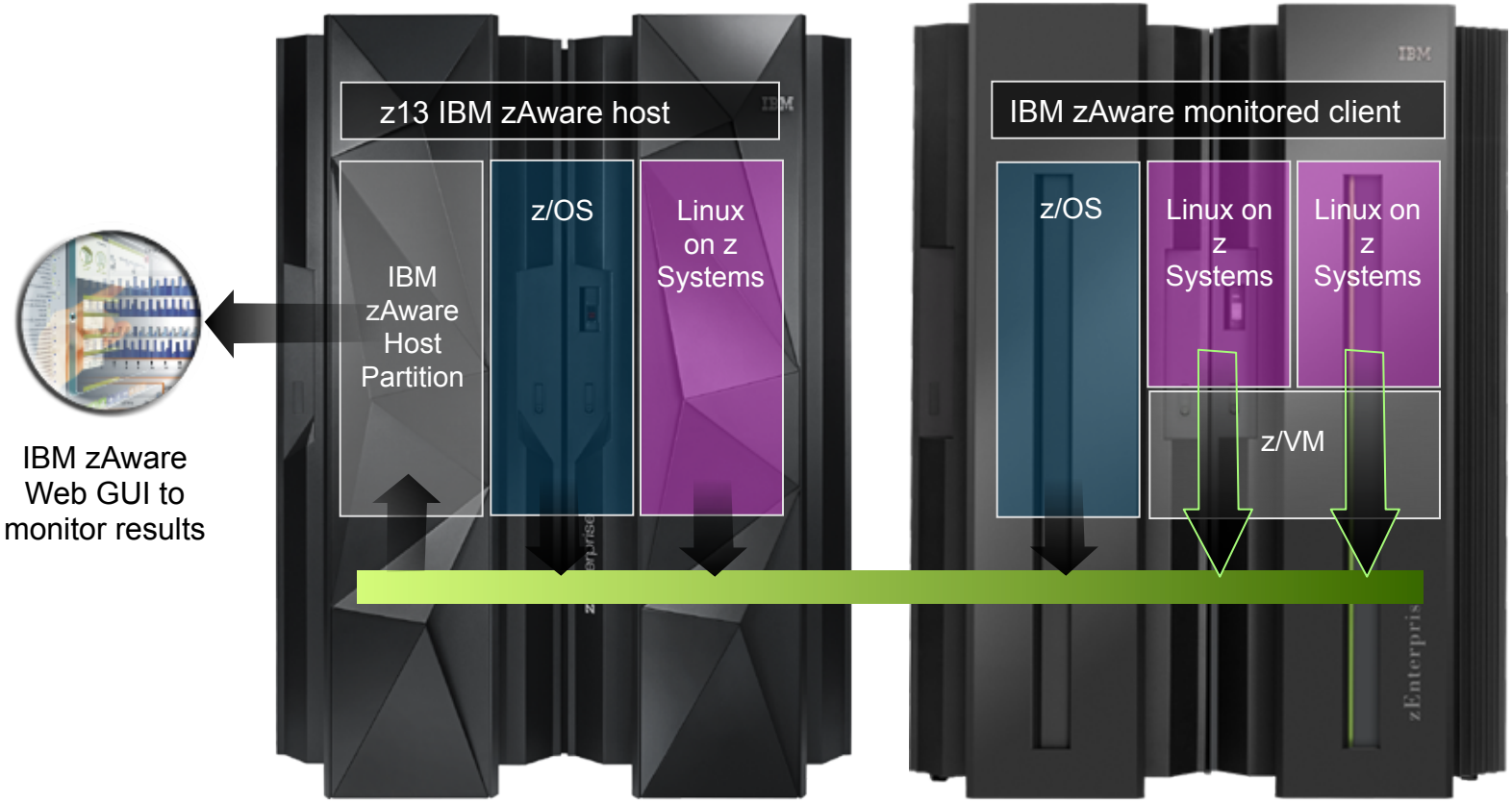
Rack Mounted Support Element

- SE RAS Improvements
  - ECC Memory
  - Truly redundant physical networks (N+1)
    - Laptops use single physical networks for SE networking requirements (HMC Network, PSCN, INMN).
    - Supports 1 Gbps
    - Redundant physical networks
  - Redundant power modules (N+1)
    - SEs continue to run:
      - SCH failure
      - Power module failure
    - Eliminates Alternate SE switches for certain power hardware repairs

IBM zAware Version 1

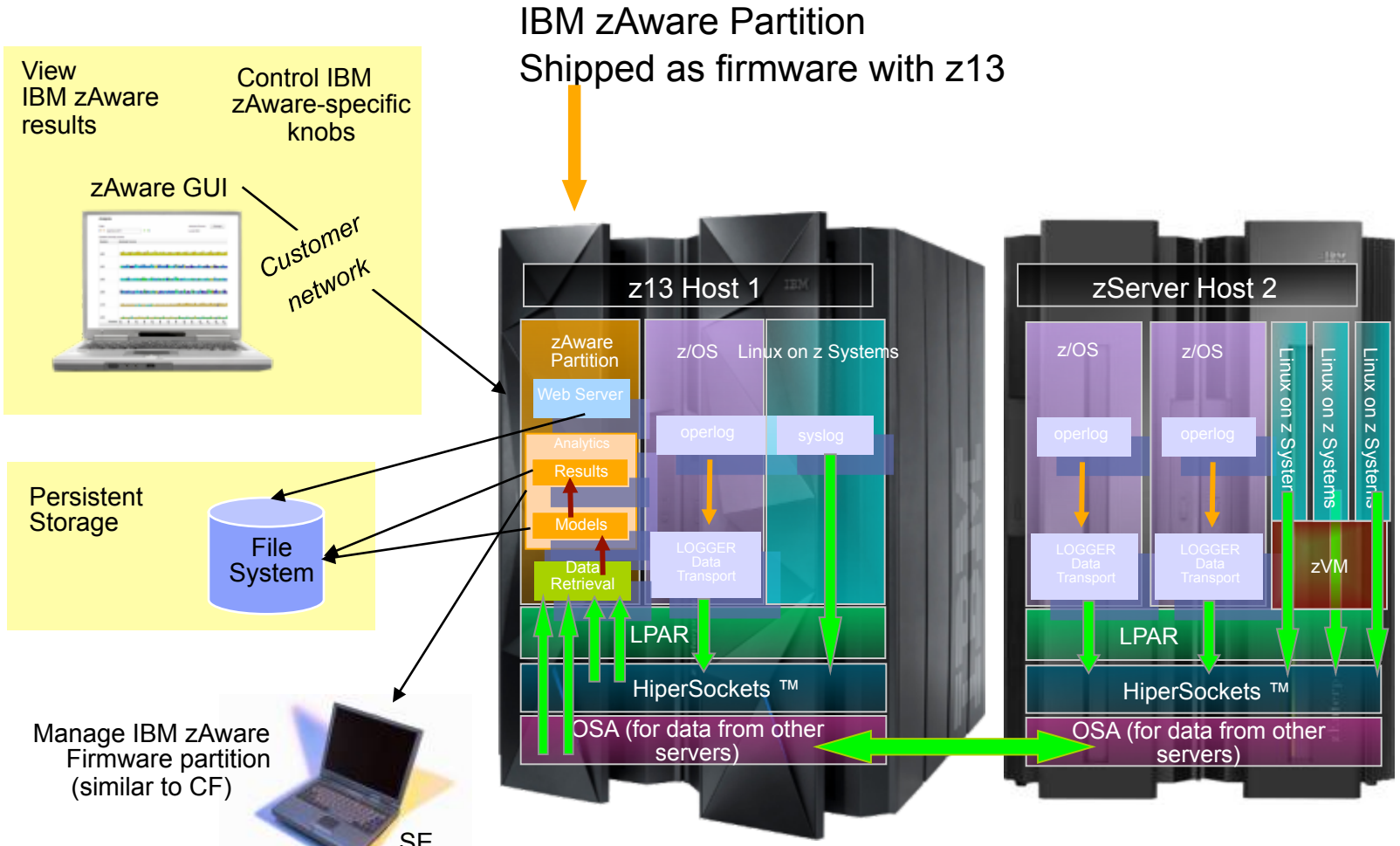
- Identify unusual system behavior of zOS images
- Proactively surface anomalies in z/OS operlog

IBM zAware V2.0 - Analyze z/OS and Linux on z Systems



- Identify unusual system behavior of Linux on system z images
- Monitors *syslog** from guest or native image in real time
- Improved analytics for z/OS message logs
- Upgraded internal database for improved RAS
- Completely rewritten UI, including heat map views

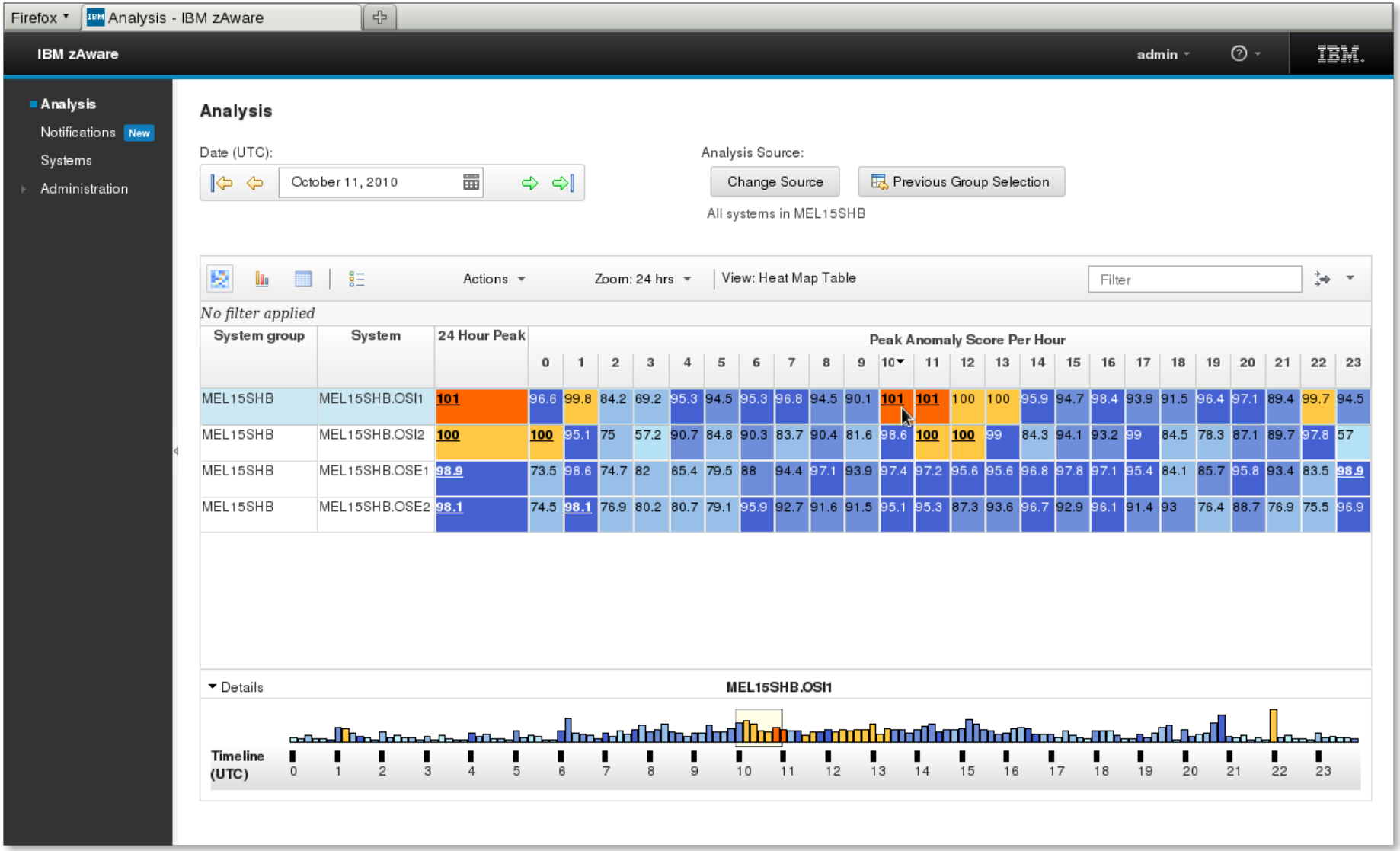
IBM zAware support for z/OS and Linux on z Systems



- Linux on z Systems system logs can now be analyzed by IBM zAware
- Upgraded analytics engine for better results on z/OS analysis
- Upgraded internal database for improved RAS
- Completely rewritten UI, including heat map views

Heat Map – All Systems in a group

- **UI with Drill down system list (ModelGroup)**



The **z13** Big Data Server

z Systems I/O Subsystem Internal Bus Interconnect Speeds (GBps)

PCIe Gen3
z13

16 GBps

PCIe Gen2
zEC12/zBC12
z196/z114

8 GBps

InfiniBand
zEC12/zBC12
z10/z196/z114

6 GBps

eSTI
z9

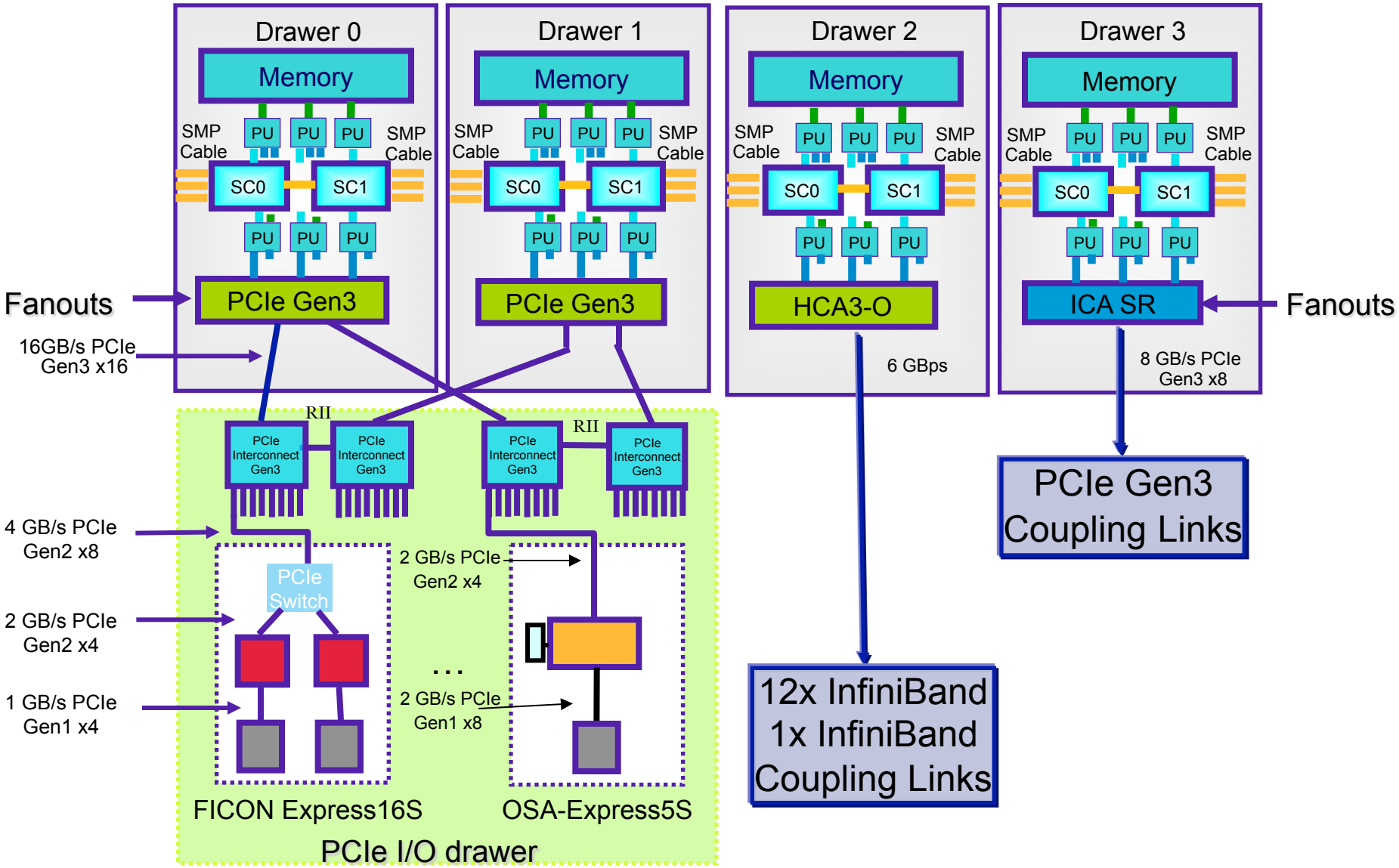
2.7 GBps

STI
z990/z890

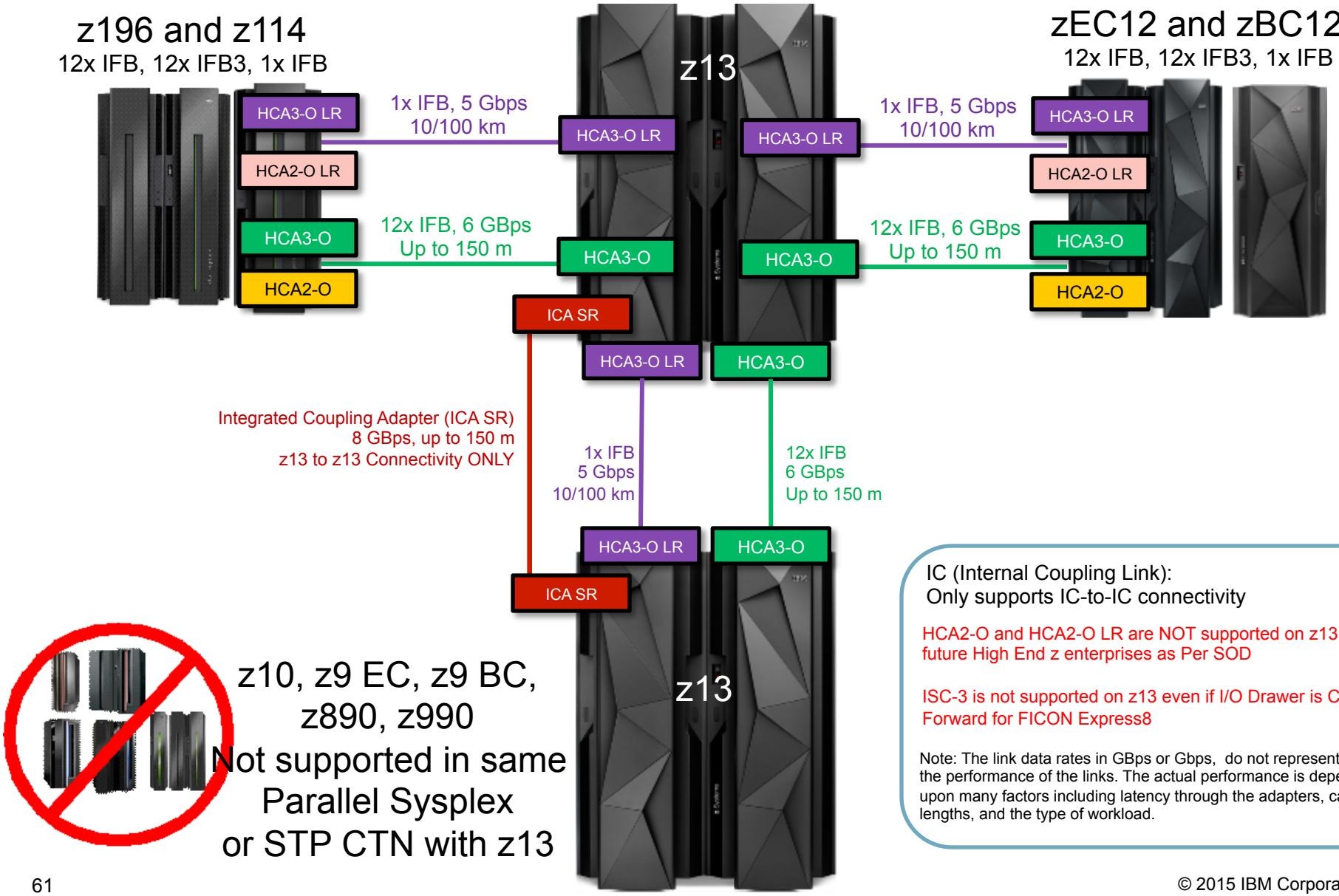
2 GBps

STI: Self-Timed Interconnect

z13 I/O Infrastructure



z13 Parallel Sysplex Coupling Connectivity



z10, z9 EC, z9 BC,
z890, z990
Not supported in same
Parallel Sysplex
or STP CTN with z13

IC (Internal Coupling Link):
Only supports IC-to-IC connectivity

HCA2-O and HCA2-O LR are NOT supported on z13 or future High End z enterprises as Per SOD

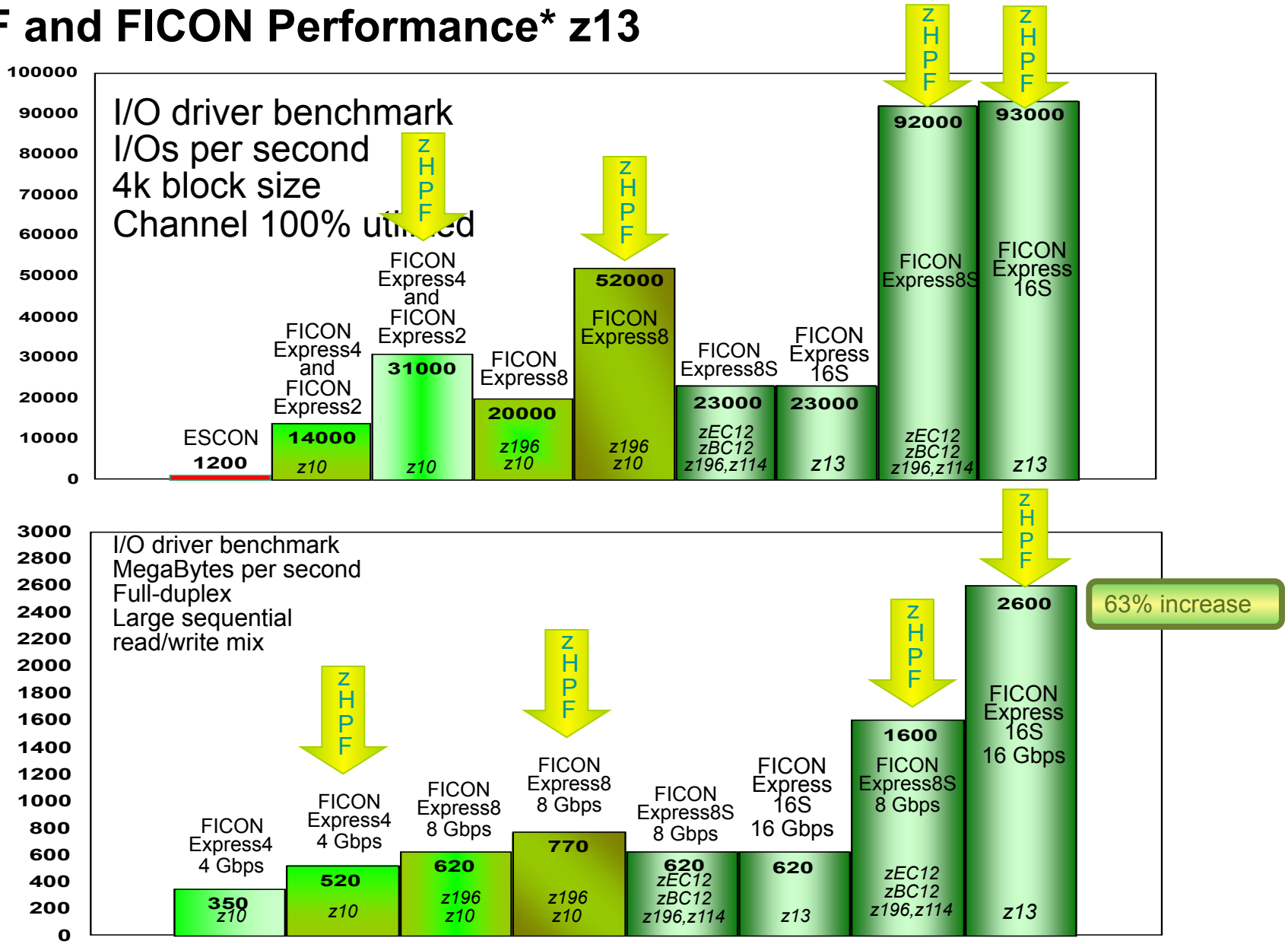
ISC-3 is not supported on z13 even if I/O Drawer is Carried Forward for FICON Express8

Note: The link data rates in GBps or Gbps, do not represent the performance of the links. The actual performance is dependent upon many factors including latency through the adapters, cable lengths, and the type of workload.

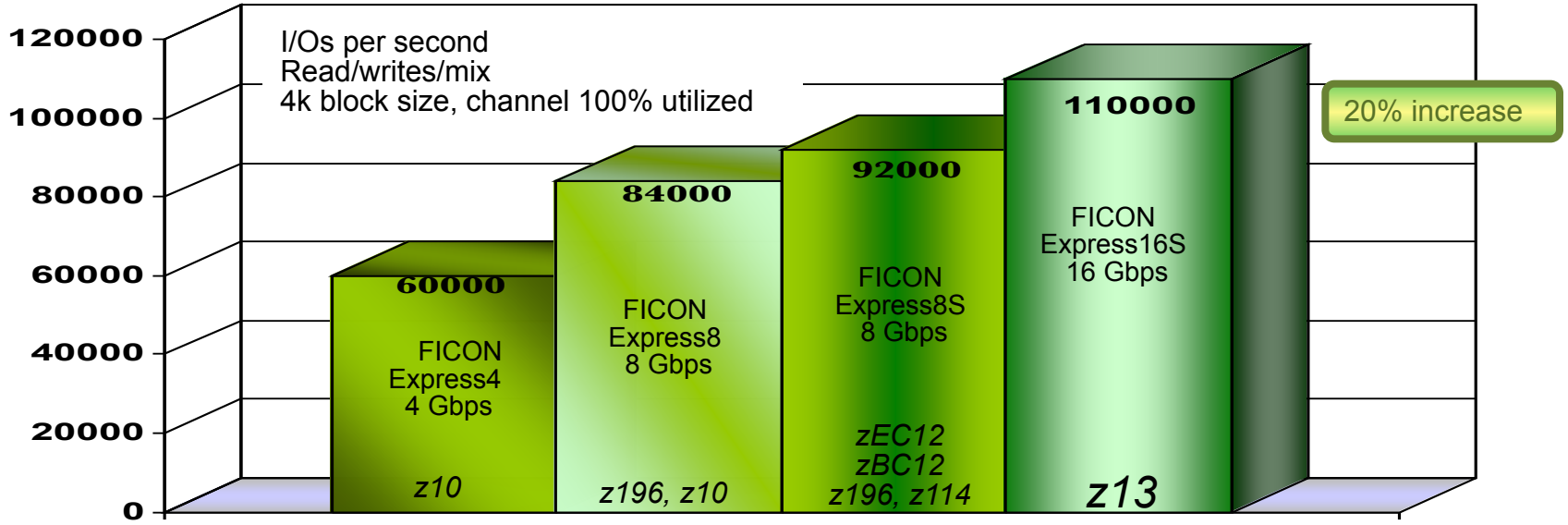
New FICON Function for z13

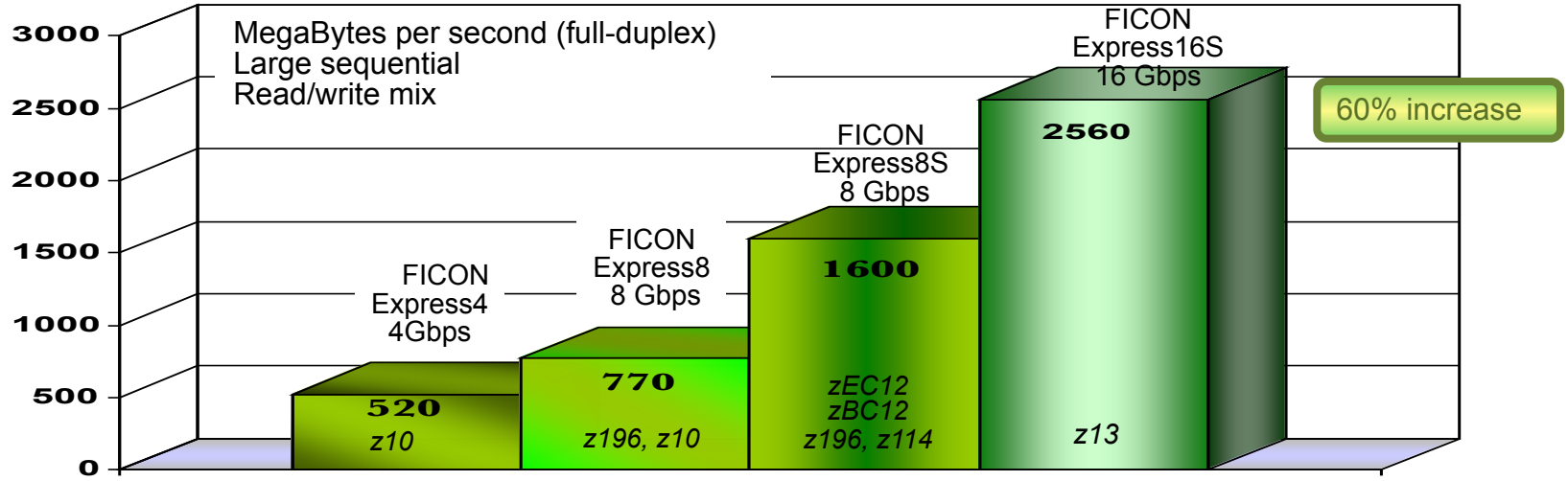
- **16 Gbps Link Speeds (March 9, 2015)**
  - Designed to reduce I/O latency to improve response time for performance-critical middleware and to shrink the batch window required to accommodate I/O bound batch work
- **6th Logical Channel Subsystem (March 9, 2015)**
  - Up to 85 Logical Partitions: More flexibility for server consolidation
- **4th Subchannel Set (March 9, 2015)**
  - Simplifies I/O configurations for a 2nd synchronous copy of data
  - With multi-target PPRC, can do HyperSwap and still maintain synchronous copy for 2nd HyperSwap
- **Preserve Virtual WWPNs for NPIV configured FCP channels**
  - Designed to simplify migration to a new-build z13 (March 9, 2015)
- **32K devices per FICON channel (March 9, 2015)**
  - Up to 85 Logical Partitions: More flexibility for server consolidation
- **zHPF Extended I/O execution at Distance (June 26, 2015)**
  - Up to 50% I/O service time improvement for remote write
  - Designed to help GDPS HyperSwap configurations with secondary DASD in remote site
- **FICON Dynamic Routing (September 25, 2015)**
  - Designed to allow ISL sharing by FC and FCP traffic to optimize use of ISL bandwidth in the SAN fabric for both types of traffic
- **Forward Error Correction Codes (September 25, 2015)**
  - Designed to addresses high bit-error rate on high frequency (>= 8Gb/s) links
  - Estimated equivalence to doubling optical signal power
- **SAN Fabric I/O Priority (September 25, 2015)**
  - Extends z/OS WLM policy into the SAN fabric
  - Gives important work priority to get through SAN traffic congestion (e.g. after SAN hardware failures)

zHPF and FICON Performance* z13



FCP Performance* for z13

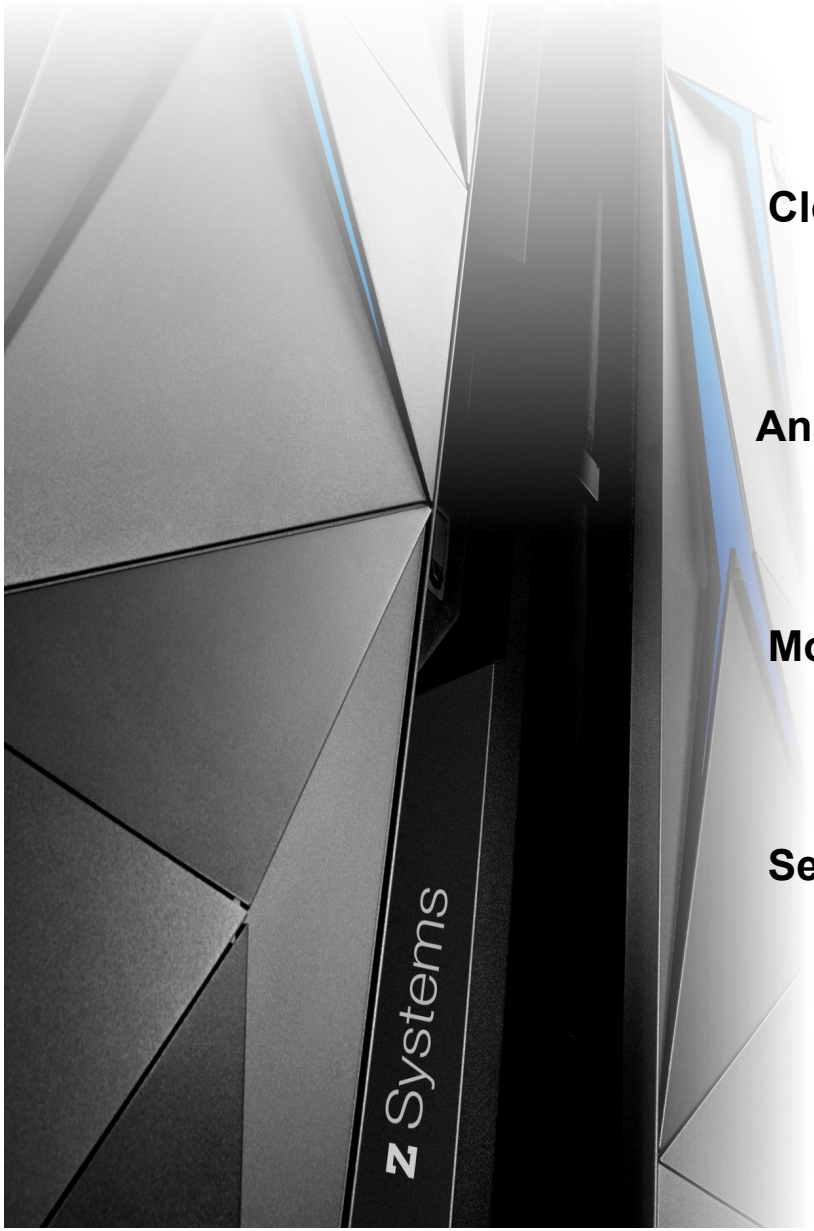




*This performance data was measured in a controlled environment running an I/O driver program under z/OS. The actual throughput or performance that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload processed.

z13 Performance - Results and Insights

The all new IBM z13: Excel in Digital Business Against Competition



Cloud

Enable superior Cloud services at **up to 32%** lower cost than x86 Cloud and **up to 60%** less than Public Cloud over three years

Analytics

Deliver insights **up to 17x** faster and with **13x** better price performance than closest competitor

Mobile

Deliver **up to 36%** better response time, **up to 61%** better throughput, and **17 to 37%** lower cost per mobile transaction

Security

Accelerate speed of encryption **up to 2X** over the zEC12 to help protect the privacy of data throughout its life cycle

The all new IBM z13: Pushing the boundaries of system innovations

Up to 10TB RAIM Memory delivers up to 50% better response time

Accelerated Analytics for Numeric-Intensive Workloads with Single Instruction Multiple Dataset (SIMD)

30% Better Capacity for Linux and Java with Simultaneous Multi-Threading (SMT)

Specialty Engines: zIIPS, IFLs, and ICFs to optimize performance across diverse workloads

Crypto Express5S providing dedicated cryptographic processing for security of transactions and data, 2x faster

Up to 141 Processor Cores with 5GHz performance and unprecedented scales for data and transaction growth

Up to 320 Separate Channels of Dedicated I/O for massive data and transaction throughput

Up to 17x Faster Analytics than the Competition with IBM DB2 Analytics Accelerator

100's of Virtual Machines in one System with new open-standards based KVM hypervisor

zEDC accelerated data compression to reduce data transfer volumes & storage costs by up to 75%

Important links for additional information

- IBM Redbooks and Redpapers introducing the IBM z13
  - http://www.redbooks.ibm.com/redbooks.nsf/pages/z13?Open
  - Hardware, SMT, SIMD, I/O, Mobile, Cloud, Analytics, etc.
- IBM z13 Announcement Information
  - http://www-03.ibm.com/systems/z/announcement.html
- IBM z13 Overview
  - http://www-03.ibm.com/systems/z/hardware/z13_specs.html
- IBM z13 Features and Benefits
  - http://www-03.ibm.com/systems/z/hardware/z13_features.html
- IBM z13 Specifications
  - http://www-03.ibm.com/systems/z/hardware/z13_specs.html

Thank you